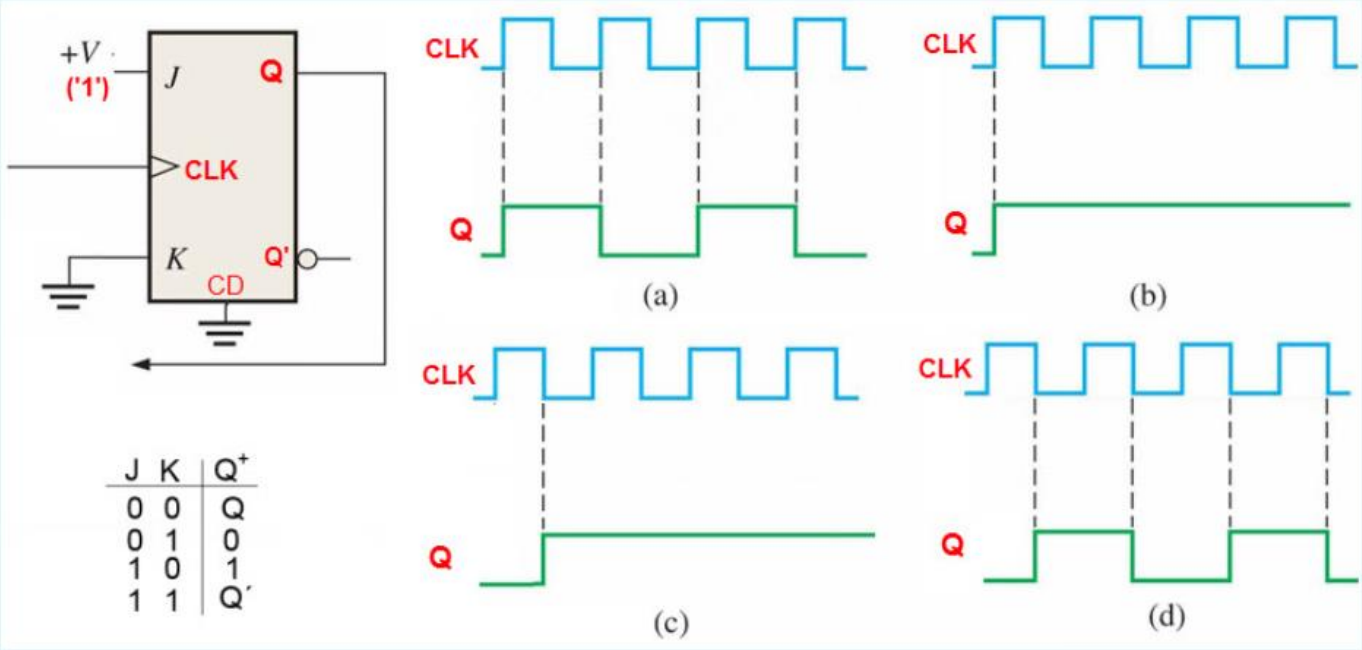
Sample P5-P6 questions

Which is the correct output of this JK flip flop connected as shown in this schematic?

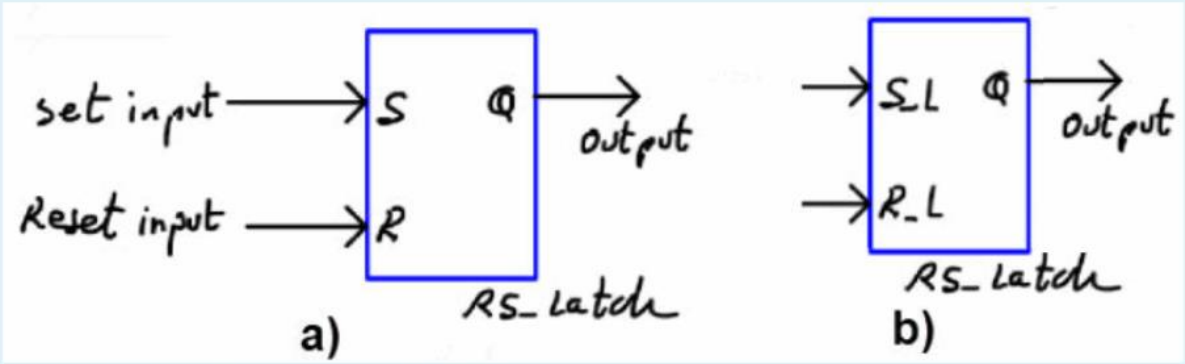


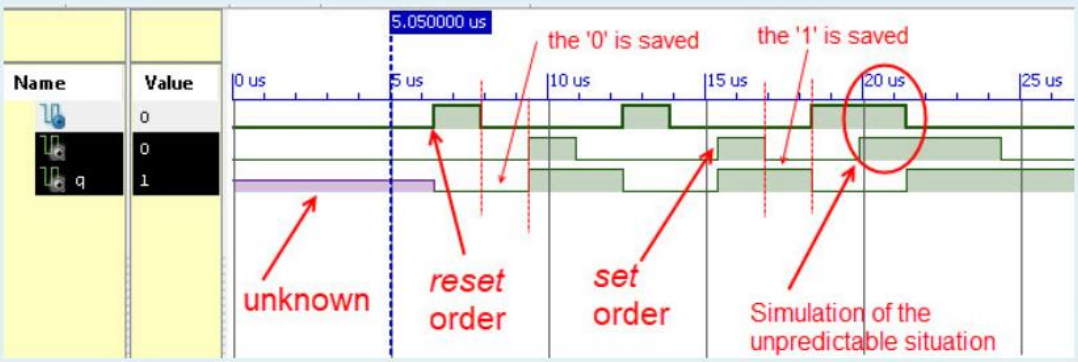
J	K	Q^+
0	0	Q
0	1	0
1	0	1
1	1	Q´

Select one:

- 1. Waveforms **d)**
- 2. Waveforms **b)**
- 3. Waveforms **c)**
- 4. Waveforms **a)**

Here we are a pair of symbols and an example of timing diagram for a 1-bit memory cell. The correct symbol that corresponds to the waveforms is the b).





Select one:

Answers

- True
- False

Examining the VHDL code below we can deduce that:

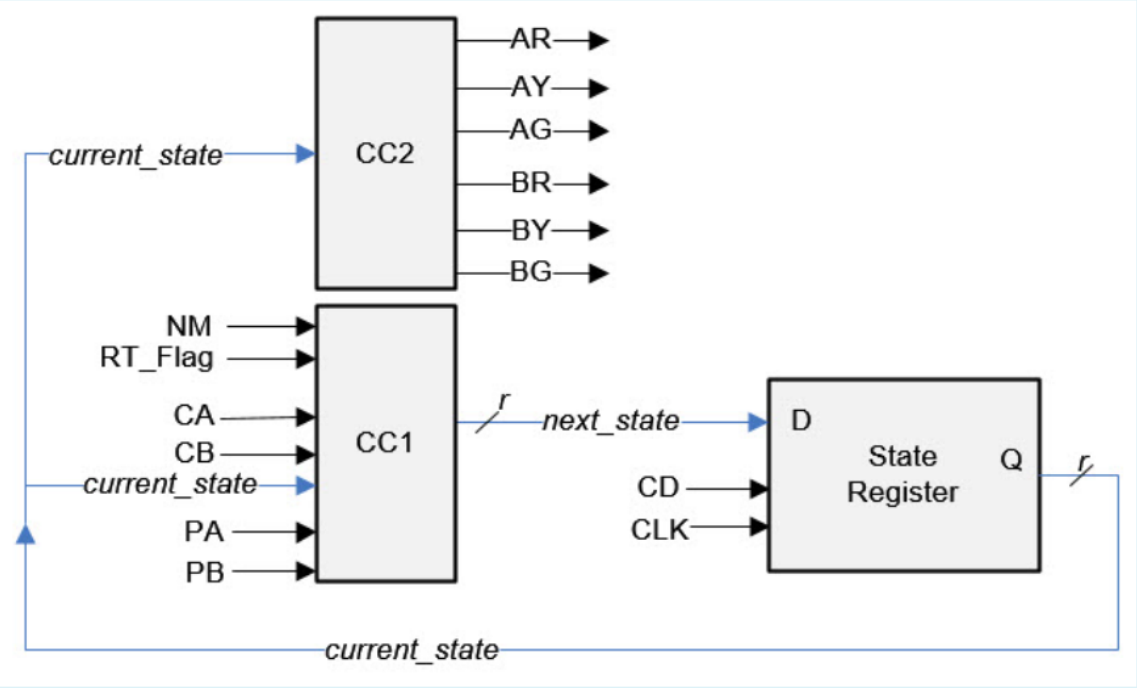
```
ARCHITECTURE structure OF circuit IS
    COMPONENT T_FF IS
        Port (
            CLK     : IN    STD_LOGIC;
            CD      : IN    STD_LOGIC;
            T       : IN    STD_LOGIC;
            Q       : OUT   STD_LOGIC
        );
    END COMPONENT;
    SIGNAL  K   : STD_LOGIC_VECTOR (3 DOWNTO 0);
BEGIN
    Chip1   : T_FF
        PORT MAP (
                CLK     => CLK,
                CD      => CD,
                T       => '1',
                Q       => K(0)
        );
    Chip2   : T_FF
        PORT MAP (
                CLK     => K(0),
                CD      => CD,
                T       => '1',
                Q       => K(1)
        );
    Chip3   : T_FF
        PORT MAP (
                CLK     => K(1),
                CD      => CD,
                T       => '1',
                Q       => K(2)
        );
    Chip4   : T_FF
        PORT MAP (
                CLK     => K(2),
                CD      => CD,
                T       => '1',
                Q       => K(3)
        );

Q  <= K;
END structure;
```

Select one:

- a. It corresponds to a synchronous circuit based on T_FF.
- b. It corresponds to an asynchronous circuit based on T_FF.
- c. Because we have no information on the entity description, we can not deduce whether the system has a common CLK for synchronicity.
- d. T_FF cannot be connected in this way, because their outputs cannot be determined.

The schematic below represents the internal architecture of a FSM to control a traffic light system. 6 outputs drive the coloured lamps and 6 inputs from several sensors and buttons determine how the machine works. The FSM has 5 states and they are coded in *one-hot*. Which one is the right answer?



Select one:

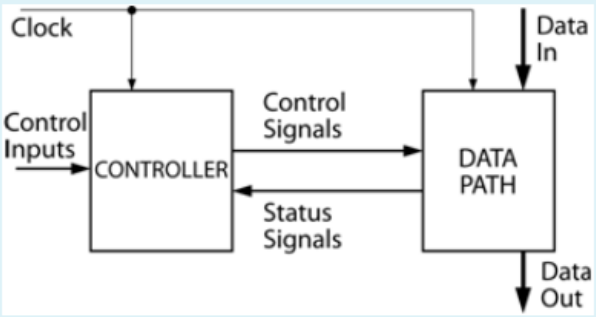
- a. It is not possible to encode the machine using *one-hot* code (00001, 00010, 00100, 01000, 10000) because binary sequential is required (000, 001, 010, 011, 100, 101).
- b. The state register contains 3 DFF; CC1 is a truth table that contains 512 combinations; CC2 has a truth table that contains 8 combinations
- c. The state register contains 5 DFF; CC1 is a truth table that contains 2048 combinations; CC2 has a truth table that contains 32 combinations.
- d. The state register contains 5 DFF; CC1 is a truth table that contains 512 combinations; CC2 has a truth table that contains 64 combinations.

CSD.

Example questions for the P7-P8 questionnaire

In datapath there are registers to save operants and results, an arithmetic and logic unit (ALU) and other combinational circuits.

The function of the status signals from the datapath to the controller FSM is to inform about the result of the operations (flags), for instance zero, carry out, negative, overflow, division by zero, etc.

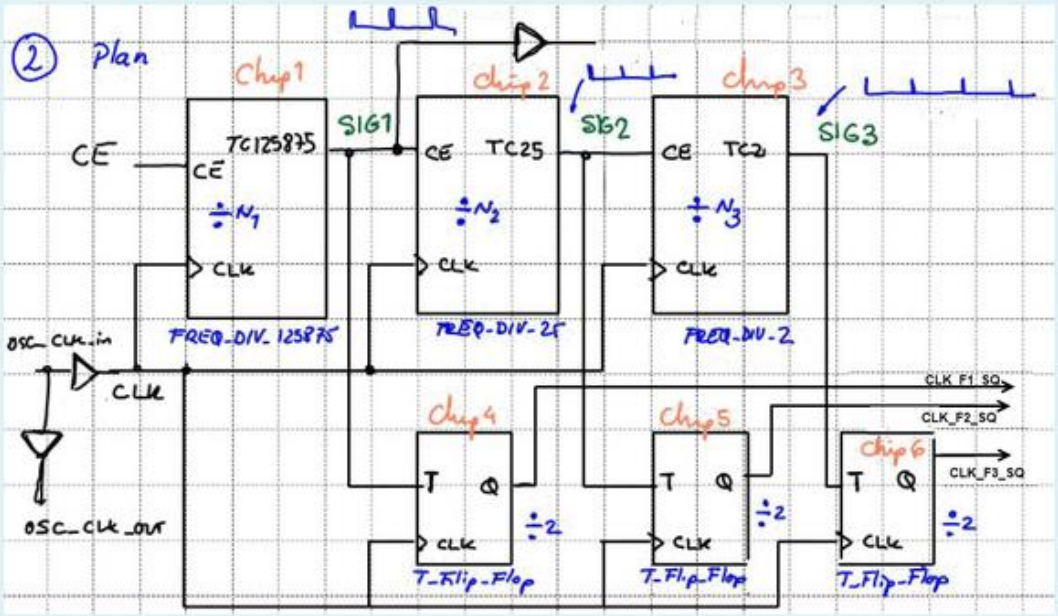


Select one:

Answers

- (•) True
- ( ) False

A *CLK_generator* circuit sketch is presented below. Which is the frequency of the output **CLK_F1_SQ** when applying an oscillator input of 100.7 MHz ?

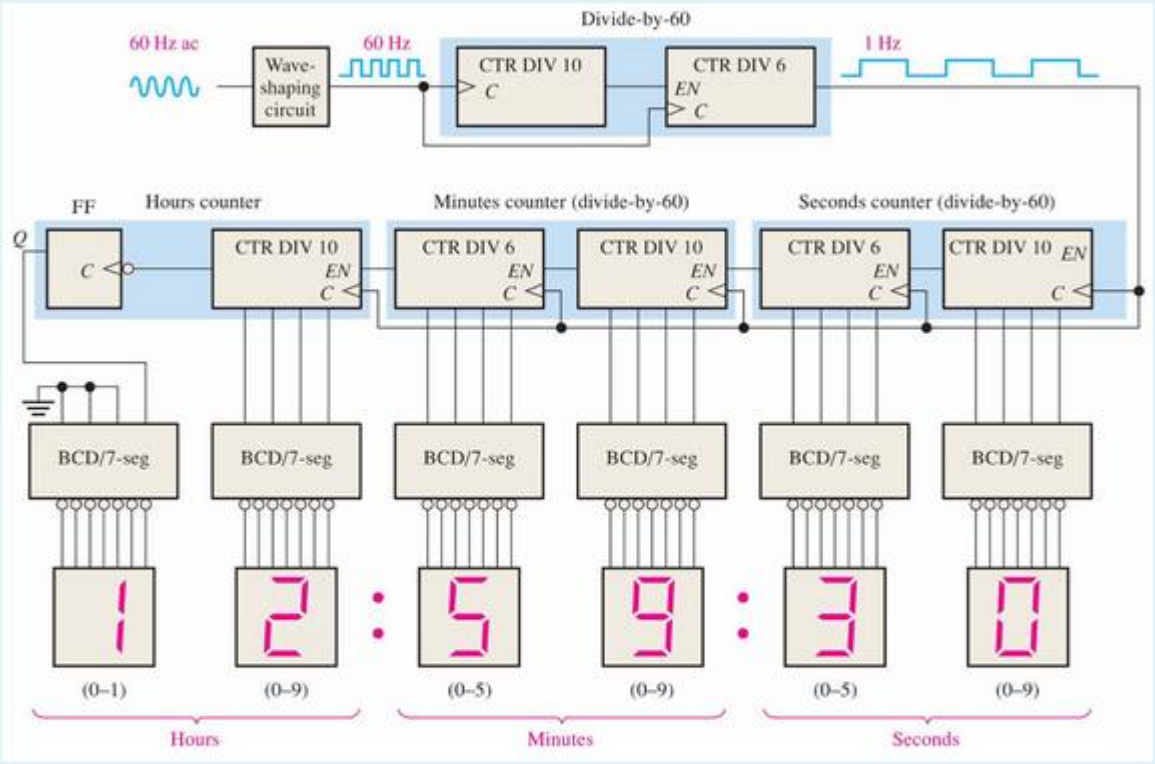


Select one:

- ( ) a. 1 Hz
- ( ) b. 25 Hz
- ( ) c. 800 Hz
- (•) d. 400 Hz

This is a schematic copied from the book T. L. Floyd, Digital Fundamentals, 9th ed., Prentice Hall, 2006. It is a design of a real-time clock that has HH:MM:SS BCD outputs. The names of the components and signals has not been adapted to our CSD naming style, but they are very similar. The wave-shaping circuit is analogue.

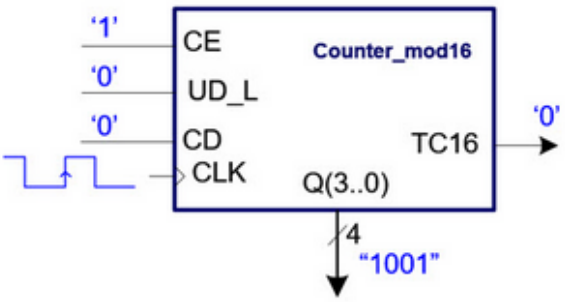
The question, after inspecting the circuit, is: how many D-FF it contains?



Select one:

- a. The circuit contains **59** data registers D-FF
- b. The circuit contains **14** data registers D-FF
- c. The circuit contains **26** data registers D-FF
- d. The circuit contains **192** data registers D-FF

With respect to the *Counter_mod16* in the picture below, which is the next state after the CLK's rising edge?



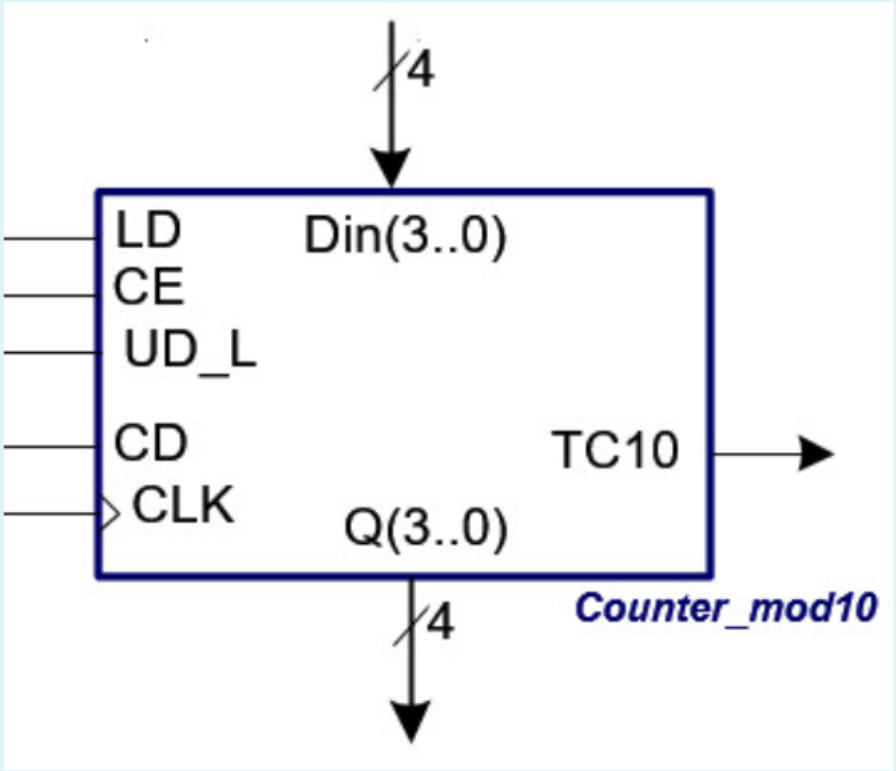
CE	UD_L	Q⁺	Synchronous operation after the CLK's rising edge
0	x	Q	Do nothing (inhibit)
1	1	$(Q+1)_{mod16}$	Up counting in binary
1	0	$(Q-1)_{mod16}$	Down counting in binary

TC16 = '**1**' when CE = '1' *and* [(Q = 15 *and* UD_L = '1') *or* (Q = 0 *and* UD_L = '0')]; '0' otherwise

Select one:

- (●) a. "1000"
- ( ) b. "1011"
- ( ) c. "1001", because the system is disabled or inhibited
- ( ) d. "1100"

Using and interconnecting 3 universal counters modulo 10 (*Counter_mod10*) like the one depicted below and other components like logic gates, we can design many different counters. Which is the maximum modulo that can be attained when connected in cascade?



Select one:

- ( ) a. *Counter_mod100*
- (●) b. *Counter_mod1000*
- ( ) c. *Counter_mod30*
- ( ) d. *Counter_mod300*