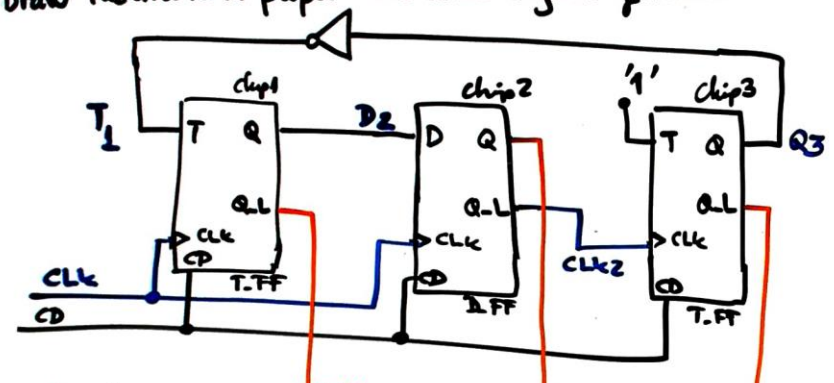
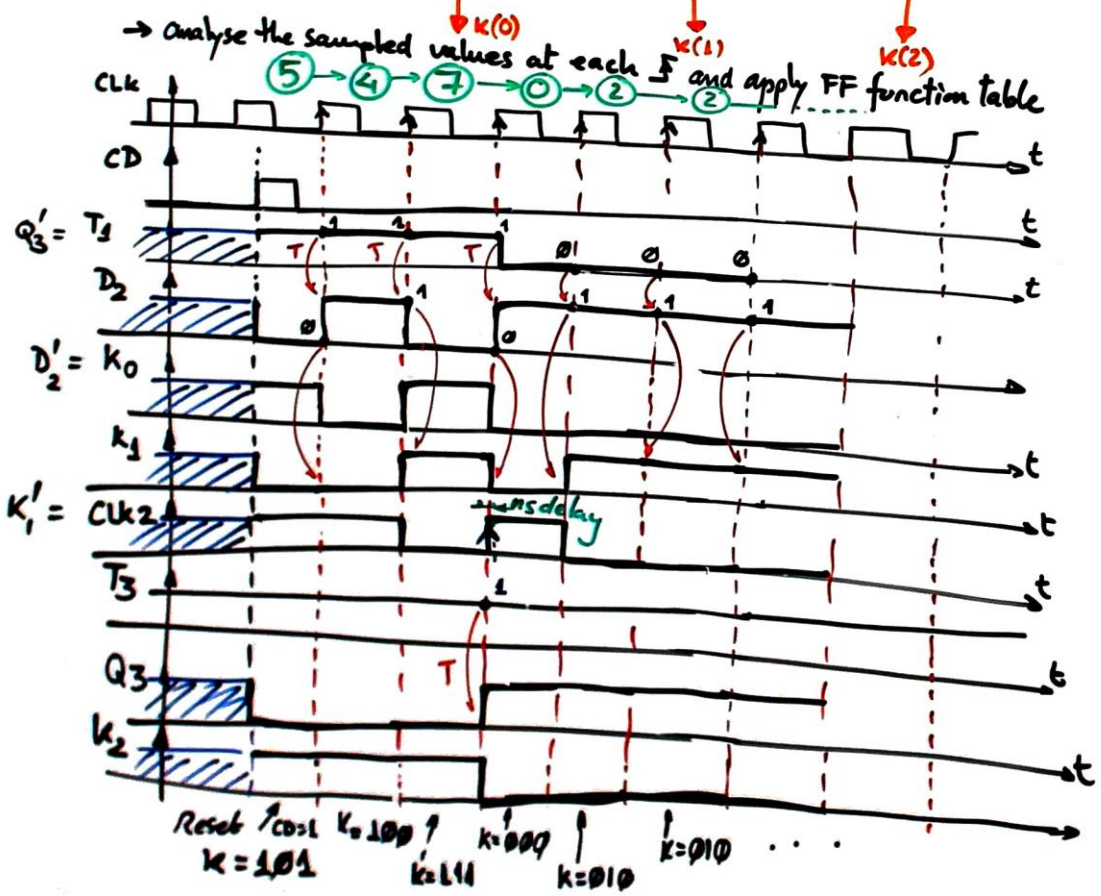
PROBLEM 1

c) → Draw the circuit in paper and name signals of interest



→ Analyse the sampled values at each $\overline{CLK}$ and apply FF function table



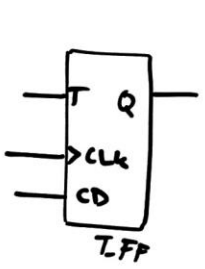
a) asynchronous circuit → FF driven by different CLK signals

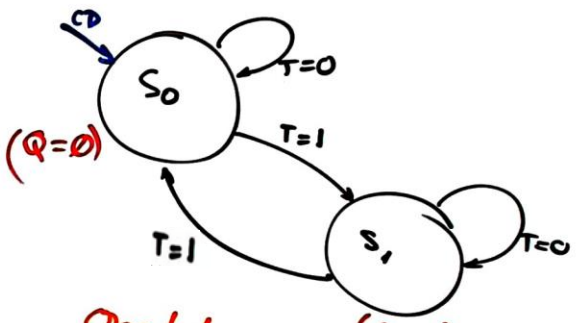
↳ delays in edge transitions and complications!

⇨ Solve the same 5→4→7→2 circuit using a canonical synchronous FSM and compare both realisations

b) T_FF.vhd, D_FF.vhd, Circuit_top.vhd, Circuit_top_tb.vhd

d)





One-hot internal current_state encoding → $S_0 = Ø1$, $S_1 = 10$ → 2 D_FF