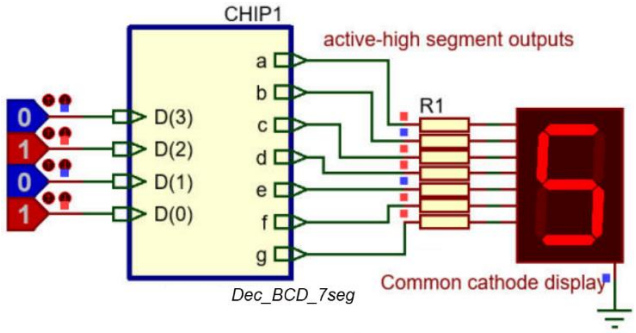
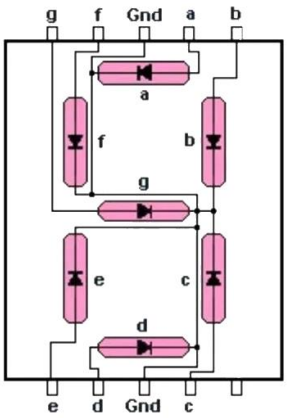
UPC. EETAC. Bachelor Degree. 2A. Digital Circuits and Systems (CSD). Grades will be available by April 11. Questions about the exam: office time.

Exam 1: (Problem 1) and [(Problem 2) or (Problem 3) or (Problem 4)] **April 4, 2024**

Problem 1 (6p)

The circuit in Fig. 1 is a BCD to 7-segment decoder to drive common cathode LED. Code "1111" generates the special symbol 'E' (error), and code "1110" generates a blank (no light).





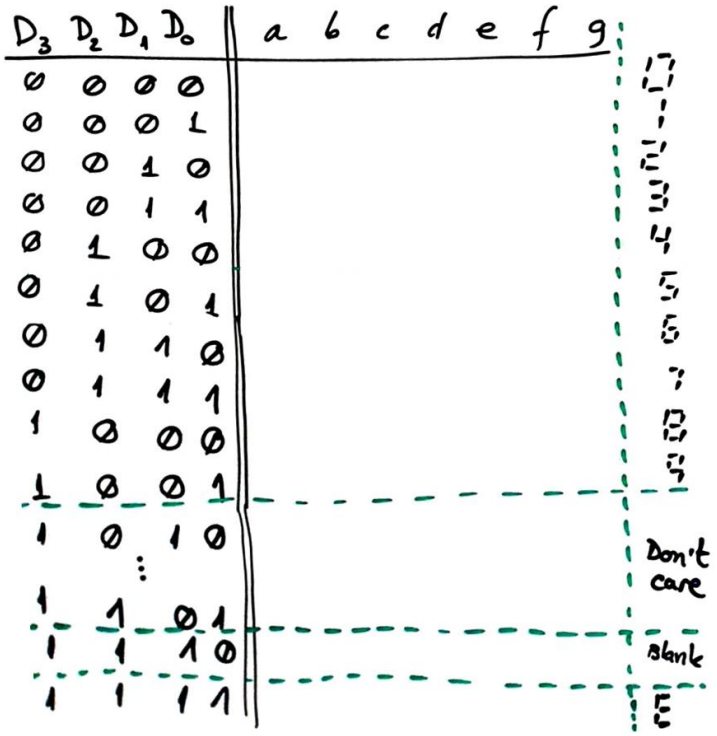


Fig. 1. *Dec_BCD_7seg* circuit.

1. Complete the truth table and write the canonical equation based on minterms of output **b** = *f*(D). Write the canonical equation based on maxterms of output **e** = *f*(D).

2. Obtain the output **d** = *f*(D) using only 2-input NAND.

3. Obtain the output **f** = *f*(D) using the method of multiplexers (MoM) and a *MUX_8.*

4. Obtain the outputs **a**, **g** using the method of decoders (MoD). Invent a decoder *Dec_4_16* using components of the same kind *Dec_2_4* and logic gates if necessary.

5. Propose a VHDL behavioural plan B for implementing the circuit.

To solve the next questions, we will imagine that one of the possible plan A circuits that we can obtain using equations is the RTL representation in Fig. 2.

6. Calculate the circuit's longest propagation time t_P and explain using a timing diagram what is the meaning of such concept. Calculate the circuit's maximum speed (number of decoding operations per second). Fig. 3 shows the characteristics of a single logic gate in classic CMOS technology.

7. Calculate the circuit's static power consumption. Calculate the dynamic power consumption imagining that all the gates are switching at maximum speed.

8. Represent the transfer function and the noise voltage margins of a CMOS gate. Using Fig. 3 data calculate the limiting resistors to bias the seven LED at I_Q = 12 mA and V_{AKQ} = 2.2 V.

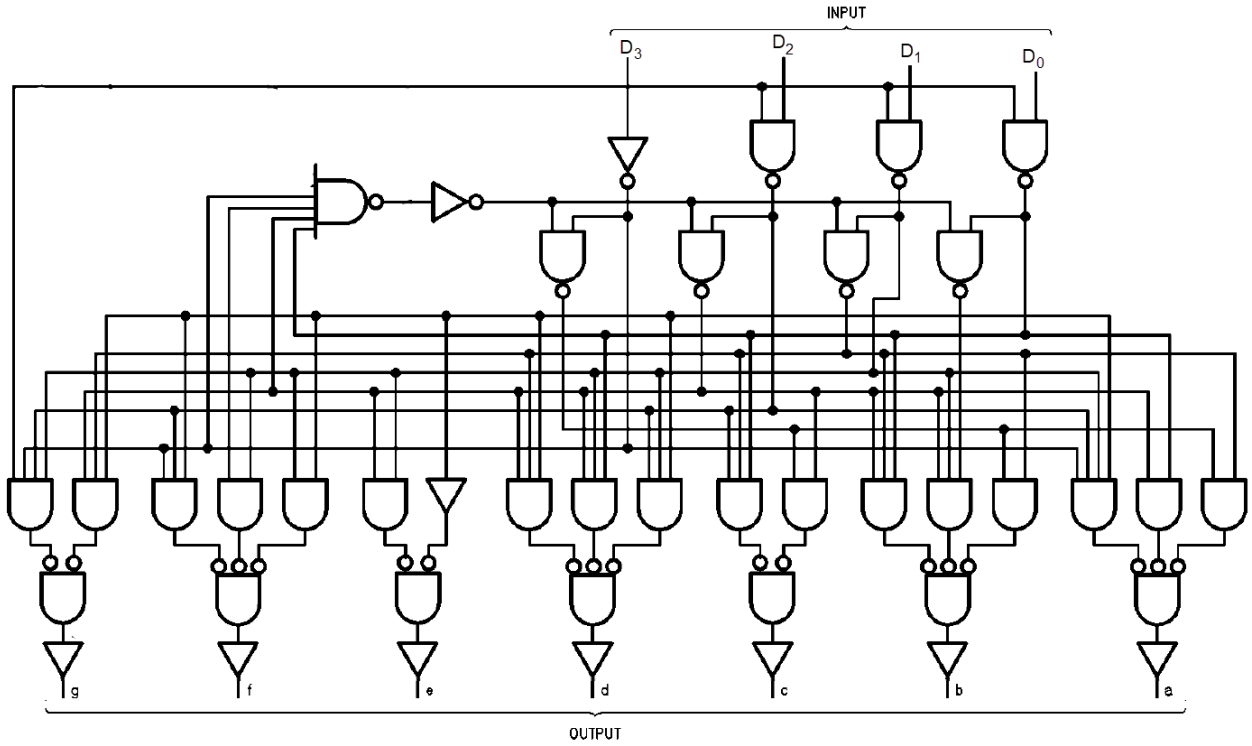


Fig. 2. A possible circuit implementation using gates.

Electrical Characteristics – Dynamic

T_A = 25°C; input t_r, t_f = 20 ns; C_L = 50 pF; R_L = 200 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	V_{DD} (V) = 5		55	110	ns

Electrical Characteristics – Static

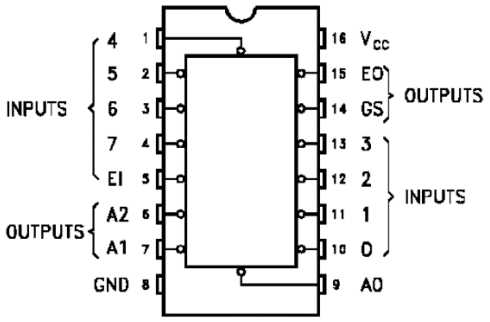
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	V_{IN} = 5 V, V_{DD} = 5 V		0	0.05	V
V_{OH}	High-level output voltage	V_{IN} = 0 V, V_{DD} = 5 V	4.95	5		V
V_{IL}	Input low voltage	V_O = 4.5 V, V_{DD} = 5 V			1	V
V_{IH}	Input high voltage	V_O = 0.5 V, V_{DD} = 5 V	4			V
I_{DDQ}	Quiescent device current	V_O = 0.5 V, V_{DD} = 5 V		0.01	0.25	µA

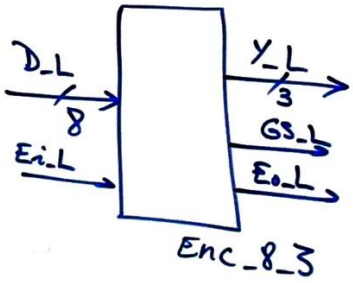
$$P_S + P_{dyn} = I_{DDQ} \cdot V_{DD} + V_{DD}^2 \cdot C_L \cdot f$$

Fig. 3. Characteristics of a single logic gate in classic CMOS technology.

Problem 2 (4p)

Our aim is to replicate in CSD the 3-to-8 line priority encoder 74HC148 represented as a classic chip in Fig. 4. We will design it using VHDL tools and plan A. All inputs and outputs are active-low. The first step is to redraw the chip's symbol and adapt signal names and the truth table in our way.





INPUTS									OUTPUTS				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	E0
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	LL	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

X: Don't Care

```
" Truth table name:
table Enc_8_3

"-------------------------------------------------------------------------------
  input Ei_L D_L7 D_L6 D_L5 D_L4 D_L3 D_L2 D_L1 D_L0
  output GS_L Y_L2 Y_L1 Y_L0 Eo_L

" Ei_L D_L7 D_L6 D_L5 D_L4 D_L3 D_L2 D_L1 D_L0    GS_L Y_L2 Y_L1 Y_L0 Eo_L
" ========================================    ==== ============== ====
  1     -    -    -    -    -    -    -    -       1    1    1    1    1  "Disabled
  0     1    1    1    1    1    1    1    1       1    1    1    1    0  "No key pressed
  0     1    1    1    1    1    1    1    0       0    1    1    1    1  "Key 0 pressed
  0     1    1    1    1    1    1    0    -       0    1    1    0    1  "Key 1 pressed
  0     1    1    1    1    1    0    -    -       0    1    0    1    1  "Key 2 pressed
  0     1    1    1    1    0    -    -    -       0    1    0    0    1  "Key 3 pressed
  0     1    1    1    0    -    -    -    -       0    0    1    1    1  "Key 4 pressed
  0     1    1    0    -    -    -    -    -       0    0    1    0    1  "Key 5 pressed
  0     1    0    -    -    -    -    -    -       0    0    1    1    1  "Key 6 pressed
  0     0    -    -    -    -    -    -    -       0    0    0    0    1  "Key 7 pressed

"-------------------------------------------------------------------------------
end
```

Fig. 4. Encoder 8 to 3 circuit truth table from the 74HC147 datasheet. Symbol adaptation and truth table captured in *minilog* ready for minimisation.

1. How long is the circuit's truth table? How many minterms contain **Y_L0**?

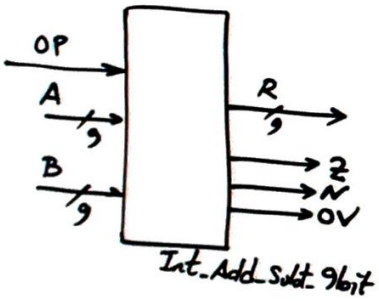
2. Represent **Eo_L** using maxterms.

3. Represent **GS_L** as a SoP. Draw the logic circuit.

4. Represent **Y_L1** as a PoS. Translate its equation into VHDL.

Problem 3 (4p)

The Fig. 5 shows the symbol of a 9-bit adder/subtractor for integer numbers coded in two's complement.



OP	A	B	R	N	Z	OV

Fig. 5. *Int_Add_Subt_9bit.*

1. How long is the circuit's truth table? What is the range of the operands? Draw an example timing diagram using the numbers and operations below. If the testbench time constant *Min_Pulse* = 232 ns, how long does it take to run the simulation of the complete truth table?

2. Perform using binary symbols ('0' and '1'), the operations for integers in two's complement (2C) indicated below to demonstrate the algorithms. Calculate as well the operation flags and discuss with is the logic behind each one.

a) (+179) – (+203)
b) (-211) – (+203)
c) (-179) + (+211)
d) (-203) + (203)

3. Propose and explain a plan C2 hierarchical internal design for the symbol in Fig. 5 capable of solving your algorithm. Design as well your components and other logic circuits that you will require. How many components will be necessary? How many VHDL files will contain this project? Deduce the number of gate-level of your circuit.

Problem 4 (4p)

Firstly, let us invent the 3-input configurable logic gate in Fig. 6 capable of performing up to four logic functions. Secondly, let us use this new *Gate_3input* as the only component to implement logic functions.

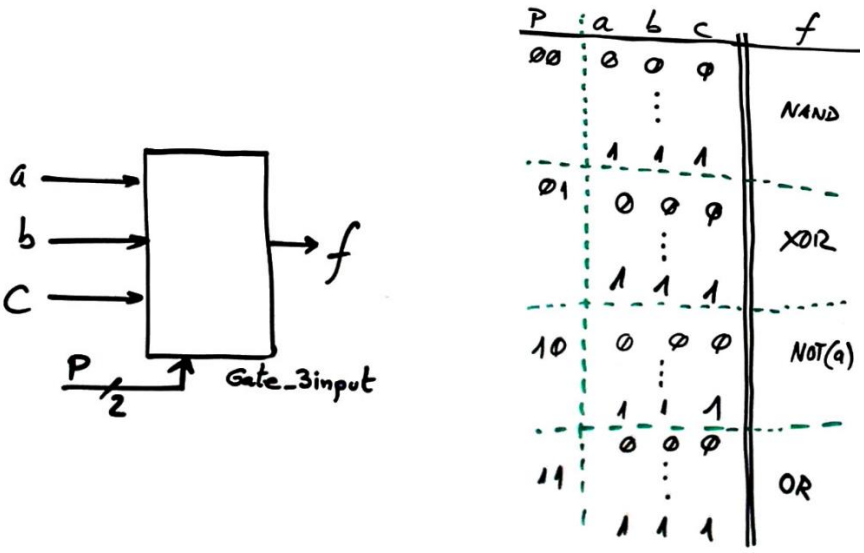


Fig. 6. *Gate_3input.*

1. Plan, develop and draw the circuit of the *Gate_3input* using the method of multiplexers (MoM) and a *MUX_4*.

2. Design the *Comb_circuit* in Fig. 7 using only *Gate_3input* components.

$$W = f(K, Q, S) = K \cdot S + S \cdot Q' + K' \cdot S' \cdot Q$$

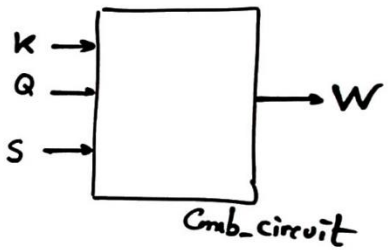


Fig. 7. Combinational circuit W = *f* (K, Q, S).

NOTE for all problems and questions: explain as clear as possible what you do and how you are inventing circuits or processing calculations. Justify your results.