Exam solution ideas

Problem 1

1. Method 1 on algebraic logic equations from any P1 project analysis. Solve the same circuit using method 2, method 3 or method 4 and compare solutions. Method 3 in LAB1.2 shows how to translate equations into VHDL.
2. Propagation delay: L4.3.
3. Power consumption L4.3 and noise margins L1.6.
4. Method 1 from any P1 project analysis.
5. Method 1 from any P1 project analysis.
6. Only-NOR and only-NOR2 circuits L1.5.

Problem 2

7-8 This is comparator for radix-2 (L3.1) and two's complement integers (L4.1) proposed in D1.17.

9-10 How to build chained comparators (L3.2, plan C2) and how to test them can be found in several example tutorial projects:

Plan C2: hierarchical structure

Comp_1bit using the MoM
Comp_4bit
Comp_10bit

Problem 3

11 Designing circuits using a single-file flat architecture in Plan B is studied in L2.3 , LAB2, and and truth table and flowcharts examples are found in many projects

Plan B: behavioural, truth table

MUX_8, Lab2

Dual_MUX_4
Dec_3_8
Hex_7seg_decoder
Enc_10_4
Dec_4_16
Quad_MUX_2 / *Quad_MUX_4*
Tank_level_meter
Bin_BCD_6bit
BCD_bin_mod40

Comp_1bit

Adder_1bit

12-13 MoD and decoder expansion examples is in L3.3.
14 MoM is also in L3.3 .
15 This plan C2 example shows how to expand multiplexers: MUX_8
16 Driving LED is found in L2.4

Problem 4

17-18-19 The highlighted project P4 shows the design and simulation of an adder/subtractor for integer numbers.

20 Gate-level and timing analyser tools are proposed in LAB4. The basics on propagation delays through a chain of multiple components is explained in L4.3.