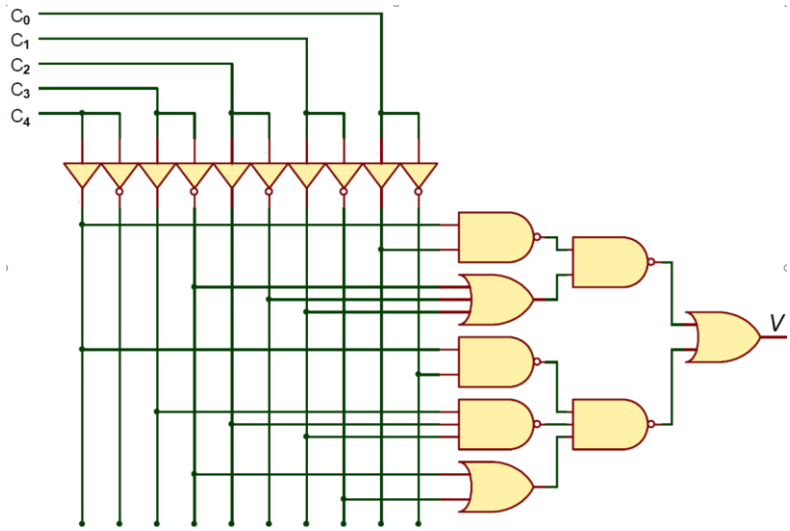
UPC. EETAC. Bachelor Degree. 2A. Digital Circuits and Systems (CSD). Grades will be available online by November 12th. Questions about the exam at office time.

Midterm exam. **November 4th, 2021**

Problem 1. (3.5p)

Analyse the digital circuit in Fig. 1. This means finding the circuit's truth table V = *f*(C(4..0)).



Characteristic	Symbol	V_{DD}	Max	Unit
Propagation Delay Time (one gate)	t_{PLH}, t_{PHL}	5.0 V	2.7	ns

V_{DD} 5.0 V 25°C		Symbol	Min	Typ #	Max
Output Voltage	"0" Level	V_{OL}	—	0.15 V	0.26 V
	"1" Level	V_{OH}	3.98 V	4.32 V	—
Input Voltage	"0" Level	V_{IL}	—	1.35 V	2.1 V
	"1" Level	V_{IH}	2.4 V	3.15 V	—

Fig. 1. Circuit to analyse. Electrical characteristics of the logic family.

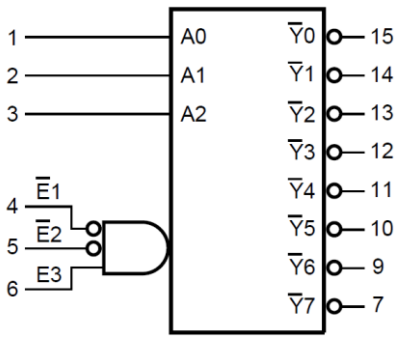
1. Draw your analysis plan using a concept map. Find the circuit's algebraic equation.
2. Apply Boolean algebra to simplify and obtain SoP (or PoS).
3. From SoP (or PoS), add missing variables to deduce the circuit's truth table.
4. Invent the circuit from SoP (or PoS) using only 2-input NOR gates.
5. Represent logic values, voltages and noise margins for this logic family.
6. If a single gate dissipates 15 µW, calculate the circuit power consumptions when V is driving ON and OFF an active-low LED with I_{DQ} = 8.5 mA and V_{AKQ} = 1.75 V. Calculate the LED's limiting resistor.
7. How fast is the circuit performing the truth table?

Problem 2. (1.5p)

Fig. 2 is an standard 74HCT138D chip, a commercial 3 to 8 decoder.

1. Rename inputs and outputs using our CSD style and draw its symbol *DEC_3_8* and truth table.
2. Design the 74HCT138D using our elemental blocks *DEC_2_4* following plan C2 based on a hierarchy of components.
3. Invent the following function T = *f*(A, B, C, D) using the method of decoders (MoD). How many VHDL files will require your circuit?

$$T = \prod M(0,\ 2,\ 5,\ 7,\ 8,\ 10,\ 13,\ 15)$$

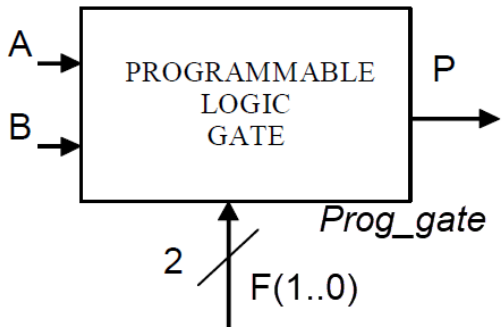


Control			Input			Output							
E1	E2	E3	A2	A1	A0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X											
X	X	L											
L	L	H	L	L	L	H	H	H	H	H	H	H	L
			L	L	H	H	H	H	H	H	H	L	H
			L	H	L	H	H	H	H	H	L	H	H
			L	H	H	H	H	H	H	L	H	H	H
			H	L	L	H	H	H	L	H	H	H	H
			H	L	H	H	H	L	H	H	H	H	H
			H	H	L	H	L	H	H	H	H	H	H
			H	H	H	L	H	H	H	H	H	H	H

Fig. 2. 74HCT138D standard chip symbol and truth table.

Problem 3. (1.5p)

We have in mind inventing the circuit in Fig. 3 for performing simple logic operations.



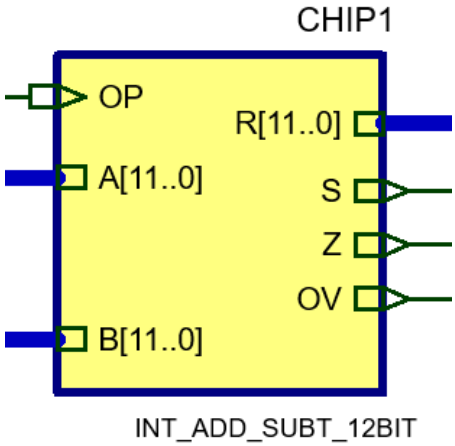
F(1..0)	P = $f(F_1, F_0, A, B)$	
00	(A + B)'	NOR
01	(A · B)'	NAND
10	A ⊕ B	XOR
11	(A ⊕ B)'	NXOR

Fig. 3. *Prog_gate* circuit symbol and logic operations.

1. How long is the circuit's truth table? How many minterms does P contain?
2. Invent the *Prog_gate* circuit using the method of multiplexers (MoM) and a MUX_2. How many VHDL files are required?
3. How fast is the circuit if the technology in Fig. 1 is used? Explain whether it is faster or slower that inventing it using a canonical circuit.

Problem 4. (3.5p)

Fig. 4 shows the arithmetic circuit *Int_Add_Subt_12bit* to perform additions and subtractions for integer numbers.



OP	**A**	**B**	**R**	OV	S	Z

Fig. 4. Arithmetic circuit for integer operands. OP = '0' → add; OP = '1' → subtract.

1. How long is the circuit's truth table? What is the range of the operands and result?
2. Solve the following integer operations determining all outputs.

```
A = - 2001          B = +2021          OP = '0'
A = - 2001          B = +2021          OP = '1'
A =(101000111110)2  B =(011000111110)2  OP = '1'
A =(101000111110)2  B =(011000111110)2  OP = '0'
```

3. Propose and complete an internal architecture for this *Int_Add_Subt_12bit* circuit based on plan C2.
4. Determine how many VHDL files contain your architecture.
5. Design flag indicators **S** (sign bit), **OV** (overflow) and **Z** (zero result) using logic gates.
6. Estimate the propagation delay of the circuit if the technology in Fig. 1 is used.
7. How long will it take to complete a full simulation at maximum speed? What tool will be used to perform such measurements?