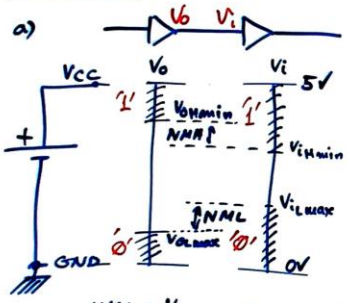
EXAM_1

Problem 1

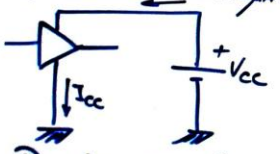
a)



$NML = V_{iL\,max} - V_{OL\,max} = 2.1V - 0.26V = 1.84V$

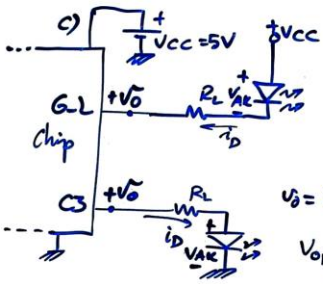
$NMH = V_{OH\,min} - V_{iH\,min} = 3.98V - 2.4V = 1.58V$

b)



$P_D = (33 \cdot 0.56\mu A) \cdot 5V = 924\,\mu W$

c)



$Vcc = V_{AK_Q} + R_L \cdot I_{D_Q} + V_{OL\,max}$

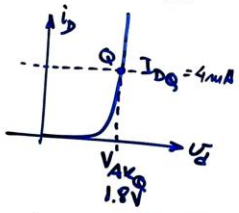
$R_L \le \frac{Vcc - V_{AK_Q} - V_{OL\,max}}{I_{DQ}} = \frac{5V - 1.8V - 0.26V}{4\,mA}$

$R_L \le 735\,\Omega$

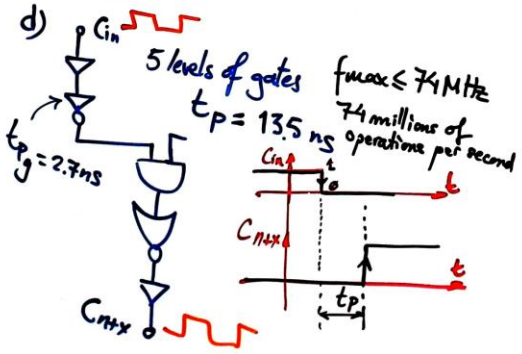
$v_D = R_L i_D + V_{AK}$

$V_{OH\,min} = R_L I_{D_Q} + V_{AK_Q}$

$R_L \le \frac{V_{OH\,min} - V_{AK_Q}}{I_{DQ}} = \frac{3.98V - 1.8V}{4\,mA} = 545\,\Omega$



d)



e) Gate-level simulation

9 inputs

$2^9 = 512$ combinations

If Min_Pulse = 13.5 ns

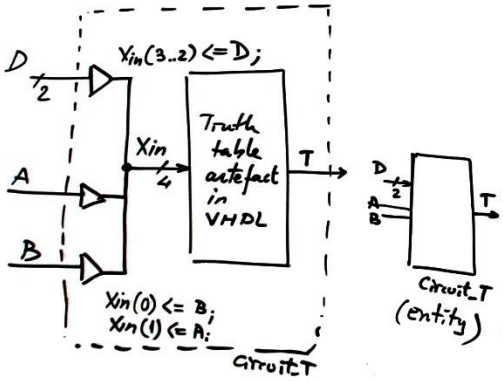
⇒ Complete test running time = 6.92 μs

Prob 2

$T = f(D_1, D_0, A, B) = TTM(1,3,6,8,10,14)$

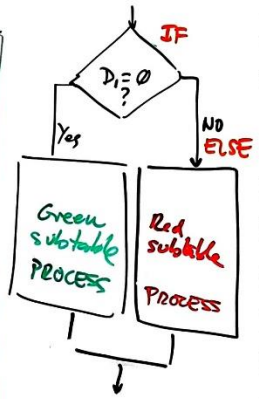
a)

This is a plan B that writes all the truth table

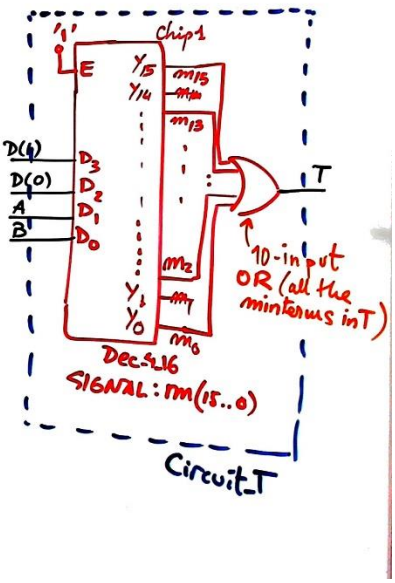


This is another plan B as a flowchart and subtruth tables

D1	D0	A	B	T
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0



b) MoD $T = f(D_1, D_0, A, B) = \sum m(0,2,4,5,7,9,11,12,13,15)$

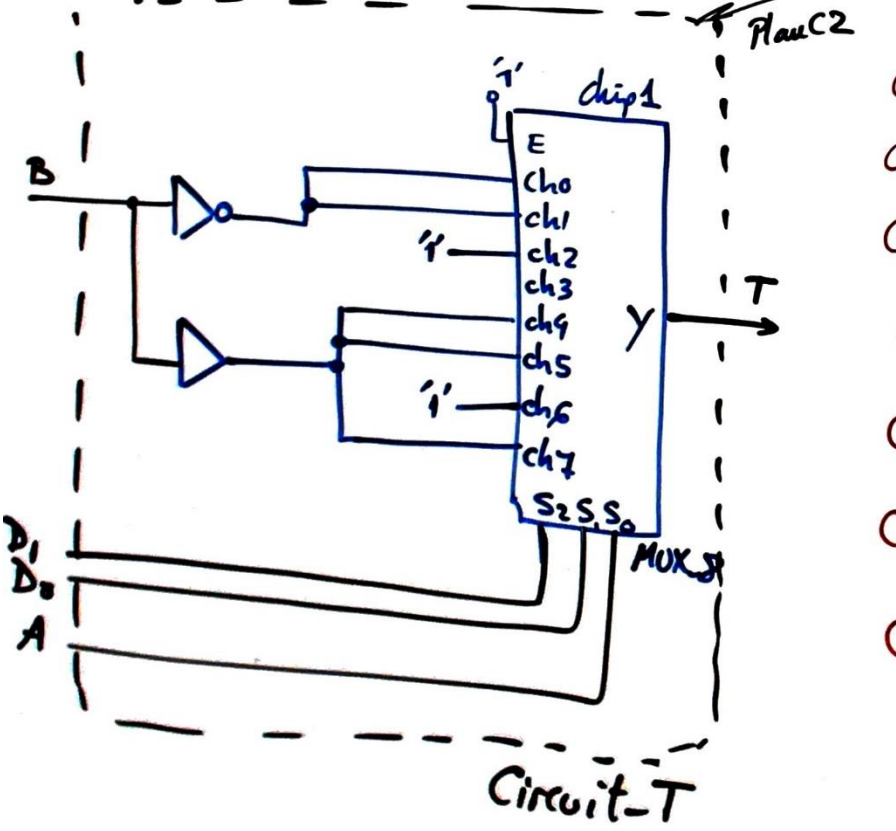


Prob_2 **c)**

$$T = f(D_1, D_0, A, B) = \Pi M(1,3,6,8,10,14)$$

c) MoM using a MUX_8

write the truth table and subdivide it into 8 sections



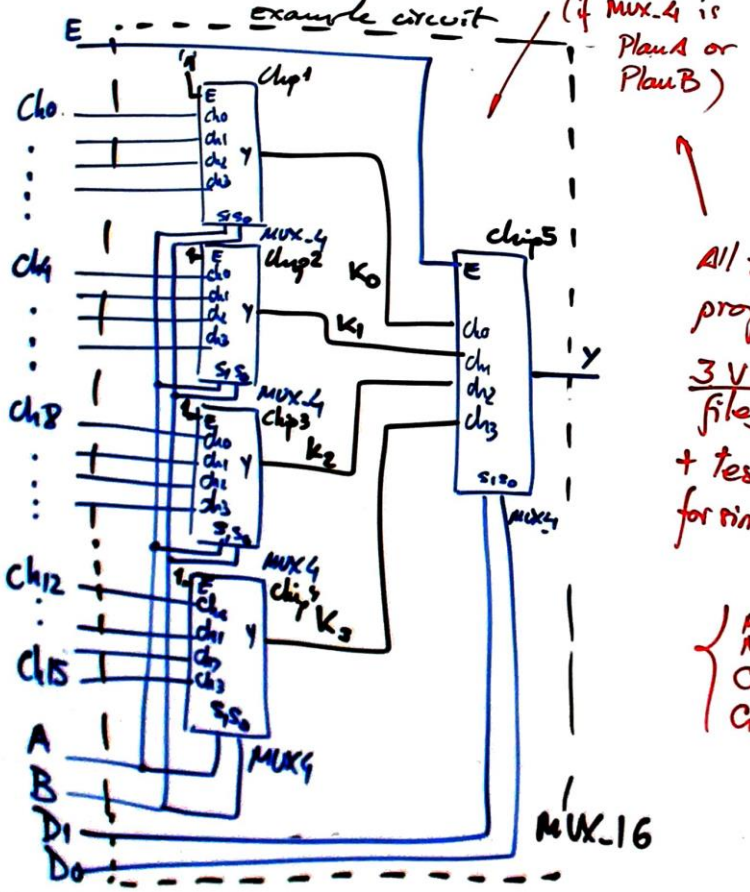
D1	D0	A	B	T	
Ch0	0	0	0	0	1	→ NOT
	0	0	0	1	0	
Ch1	0	0	1	0	1	NOT
	0	0	1	1	0	
Ch2	0	1	0	0	1	→ '1'
	0	1	0	1	1	
Ch3	0	1	1	0	0	Buffer
	0	1	1	1	1	
Ch4	1	0	0	0	0	
	1	0	0	1	1	Buffer
Ch5	1	0	1	0	0	
	1	0	1	1	1	Buffer
Ch6	1	1	0	0	1	
	1	1	0	1	1	→ '1'
Ch7	1	1	1	0	0	
	1	1	1	1	1	Buffer

Select inputs

Prob 2

$$T = f(D_1, D_0, A, B) = \Pi M(1,3,6,8,10,14)$$

d) MUX_16 using plan C2



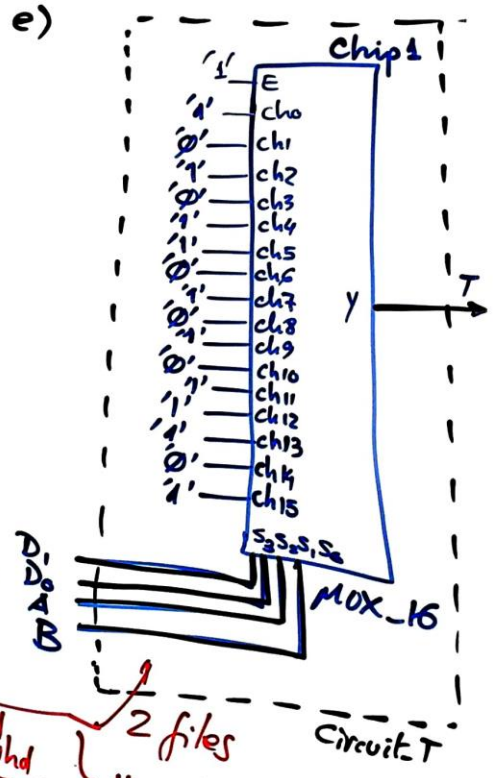
All the project:

3 VHDL files + testbench for simulation

MUX_4.vhd
MUX_16.vhd
Circuit_T.vhd
Circuit_T_tb.vhd
} 2 files

Hierarchical architecture plan C2

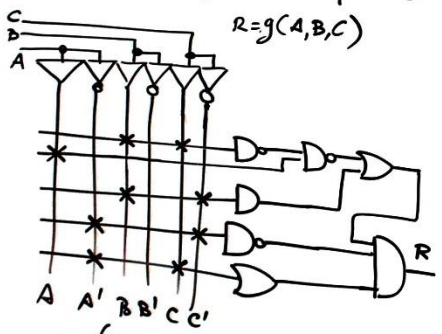
e)



Problem 3

a) Circuit's equation

$R = g(A,B,C)$



$$R = \left(\left((B \cdot C)' \cdot A\right)' + B \cdot C'\right) \cdot (A' \cdot C)' \cdot (A' + C)$$

b) Simplify

$$(A' \cdot C)' = A + C$$

$$(B \cdot C)' = B' + C'$$

$$\left[(B' + C)' + A' + BC'\right](A+C)(A'+C)$$

$$(BC + A' + BC') \cdot C$$

$$\left(B\underbrace{(C+C')}_{1} + A'\right)C$$

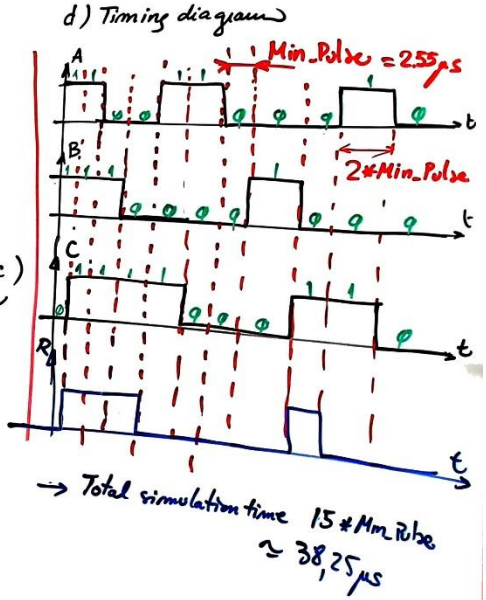
$$R\Big|_{SoP} = BC + A'C$$

c) $R = BC + A'C = ABC + A'BC + A'BC + A'B'C$

$m_7 + m_3 + m_3 + m_1$

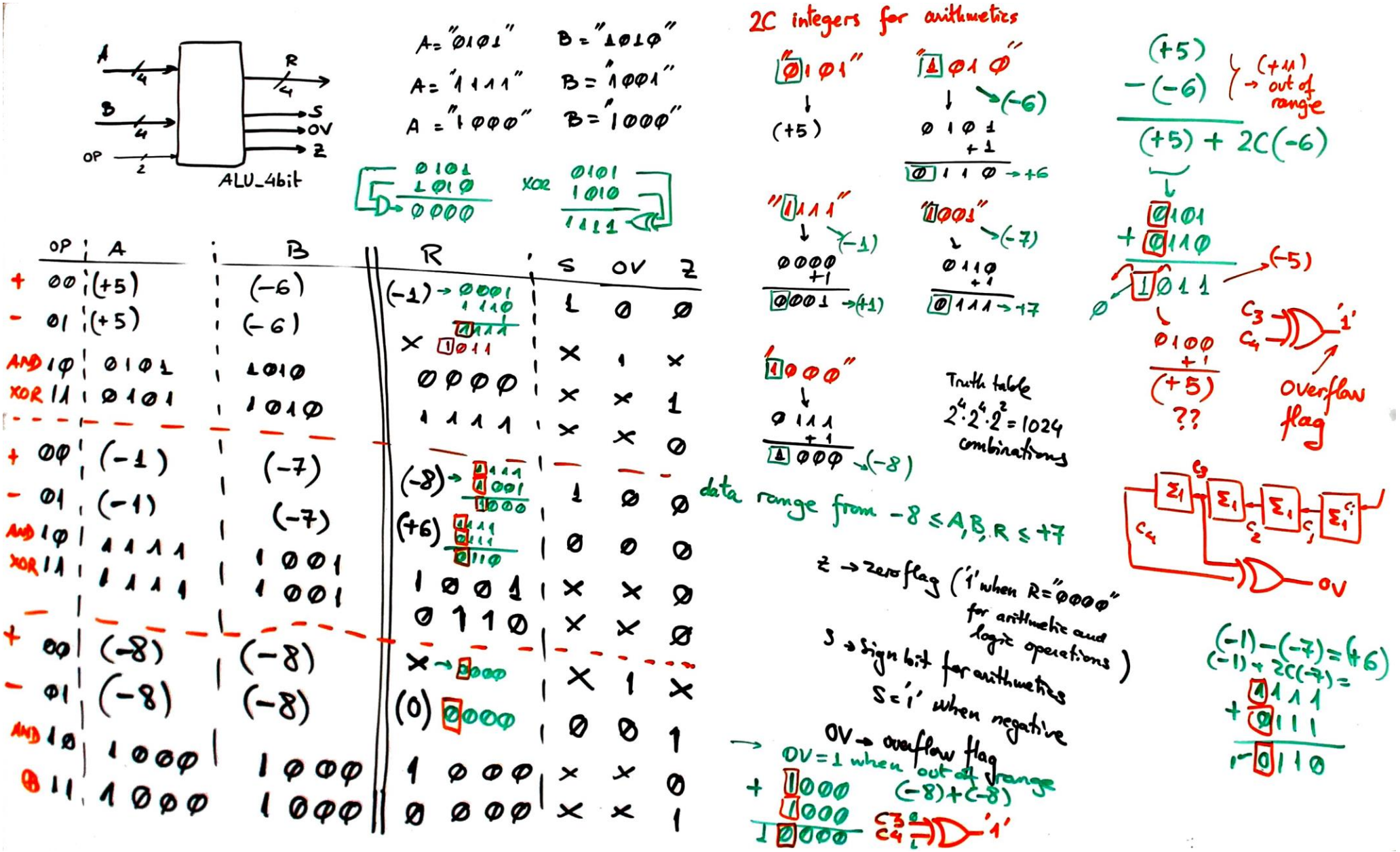
Truth table $\Rightarrow R = \sum m(1,3,7)$

d) Timing diagram



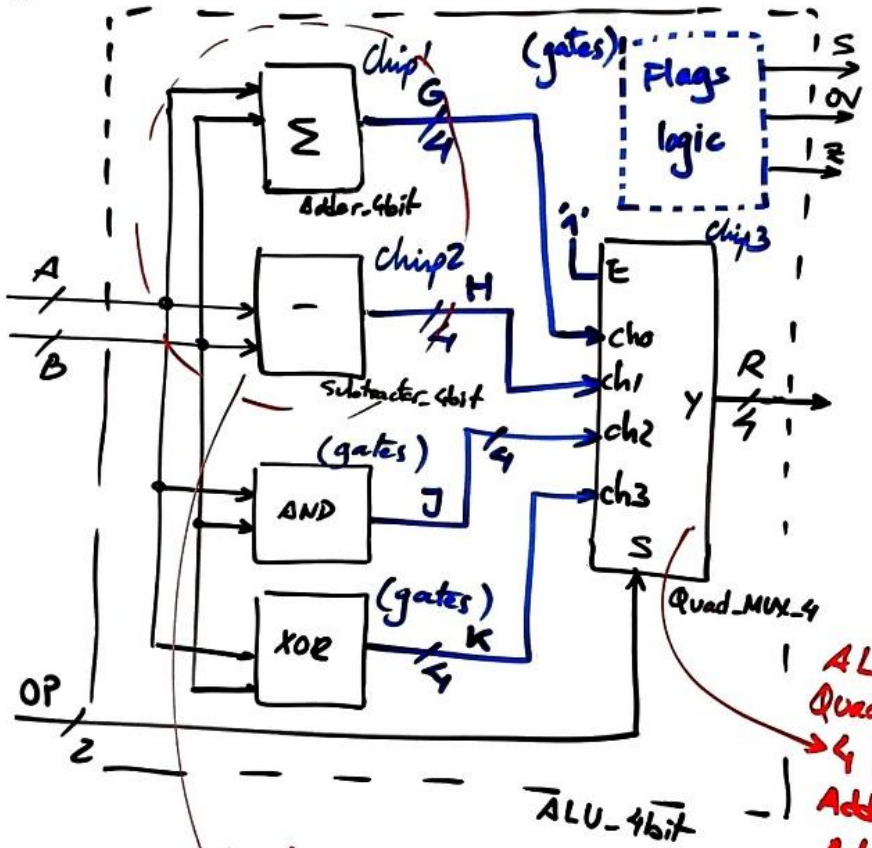
→ Total simulation time $15 * Min\_Pulse \approx 38{,}25\ \mu s$

Problem 4



OP	A	B	R	S	OV	Z
+ 00	(+5)	(-6)	(-1) → 0001 + 1110 = 1111	1	0	0
- 01	(+5)	(-6)	× 1011	×	1	×
AND 10	0101	1010	0000	×	×	1
XOR 11	0101	1010	1111	×	×	0
+ 00	(-1)	(-7)	(-8) → 1111 + 1001 = 1000	1	0	0
- 01	(-1)	(-7)	(+6) 1111 + 0111 = 0110	0	0	0
AND 10	1111	1001	1001	×	×	0
XOR 11	1111	1001	0110	×	×	0
+ 00	(-8)	(-8)	× → 0000	×	1	×
- 01	(-8)	(-8)	(0) 0000	0	0	1
AND 10	1000	1000	1000	×	×	0
XOR 11	1000	1000	0000	×	×	1

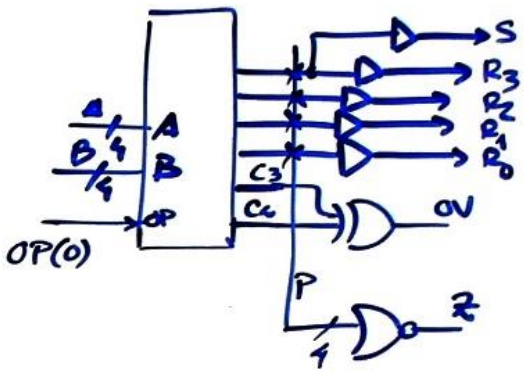
b) ALU_4bit architecture example



ALU_4bit.vhd
Quad_MUX_4.vhd
4 MUX_4.vhd
Adder_4bit.vhd
Adder_1bit.vhd
Subtractor_1bit.vhd

Can be combined in a single Int_Add_Subt_4bit using { A+B ; A+(-B)=A+2C(B) }

c) Combining Int_Add_Subt_4bit



d)

x	y	z = (x+y)(x'+y')
0	0	0
0	1	1
1	0	1
1	1	0

$$Z = \Big(\big((x+y)(x'+y')\big)'' \Big((x+y)' + (x'+y')' \Big)' \Big)'$$

only 3 NOR of 2 inputs