UPC. EETAC. Bachelor Degree. 2A. Digital Circuits and Systems (CSD). Dr F. J. Robert. Grades will be available online on November 18th. Questions about the exam at office time.

Exam 1. **November 11th, 2020**

Problem 1. (0.5p each question)

The Fig. 1 shows the internal structure (technology view) of a standard classic HCT chip with the given electrical characteristics.

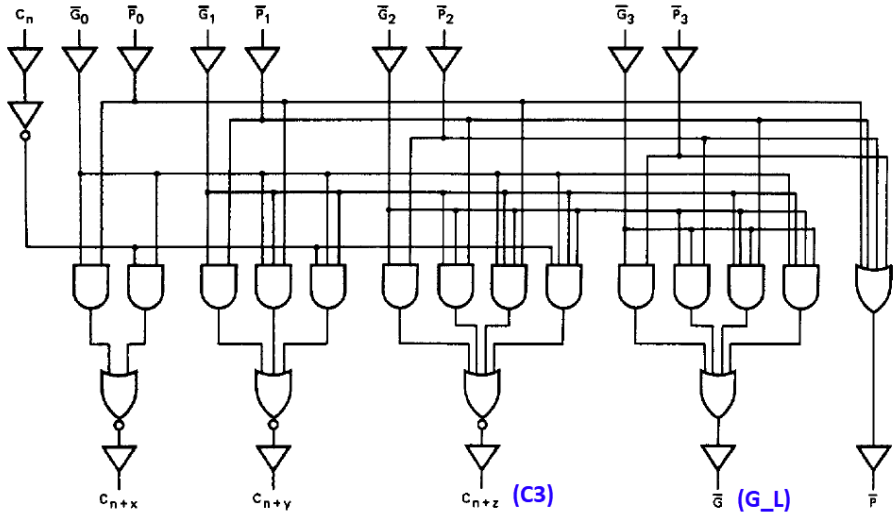
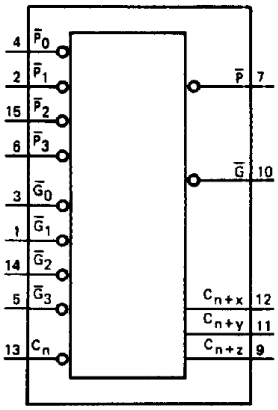


Fig. 1
Symbol, structure and electrical characteristics.



Characteristic	Symbol	V_{DD}	Max	Unit
Propagation Delay Time (one gate)	t_{PLH}, t_{PHL}	5.0 V	2.7	ns

V_{DD} 5.0 V 25°C		Symbol	Min	Typ #	Max
Output Voltage	"0" Level	V_{OL}	—	0.15 V	0.26 V
	"1" Level	V_{OH}	3.98 V	4.32 V	—
Input Voltage	"0" Level	V_{IL}	—	1.35 V	2.1 V
	"1" Level	V_{IH}	2.4 V	3.15 V	—

a) Represent logic values, voltages and noise margins for this logic family.
b) Calculate the chip's power consumption if each gate drains 0.56 µA and is powered at 5.0 V.
c) Calculate limiting resistors for a pair of LED (V_{AK} = 1.8 V, I_{LED} = 4 mA) connected at output **G_L** active-low, output **C3** active-high.
d) Which is the longest propagation path? Calculate the maximum speed of operation.
e) Which VHDL simulation allows us to measure propagation time delays in a given signal transition? What is the minimum time that it takes to simulate the entire input stimulus?

Problem 2. (0.5p each question)

The equation in Fig. 2 represents a truth table which is going to be solved in VHDL using the plan B (behavioural) and the plan C2 (hierarchical based on components).

$$\boldsymbol{T = f(D_1, D_0, A, B) = \prod \mathbf{M}(1, 3, 6, 8, 10, 14)}$$

Fig. 2
Truth table of a 4-input combinational circuit named *Circuit_T*

a) Solve the function using a plan B, a behavioural approach. Represent a schematic or flowchart and explain how to translate it into VHDL.
b) Solve the function **T** using the method of decoders (MoD).
c) Solve the function **T** using the method of multiplexers (MoM) and a MUX_8.
d) Invent a MUX_16 using components of the same kind (MUX_8, MUX_4, MUX_2) and logic gates if necessary.
e) Solve the function **T** using the method of multiplexers (MoM) and MUX_16. How many VHDL files will contain this project?

Problem 3.

a) Obtain the logic expression of the function **R**= *g*(A, B, C) of the circuit in Fig. 3. (0.5p)

b) Simplify the function to obtain a PoS or SoP. (0.5p)

c) Draw the circuit's truth table and invent another equivalent circuit based on only-NAND of two inputs. (0.5p)

d) Deduce the output **R** in the timing diagram of the circuit in Fig. 3 when the input stimulus is applied. If *Min_Pulse* is 2.55 µs, how long does it take to run all the simulation of the stimulus represented? (1p)

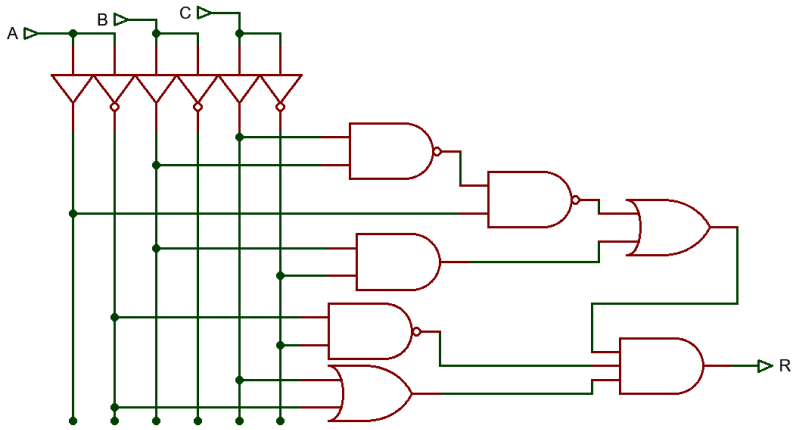
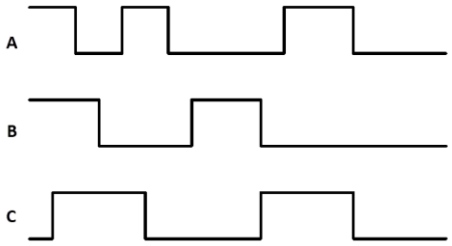


Fig. 3
Combinational circuit based on logic gates. **R** = *g*(A, B, C) and proposed stimulus file.



Problem 4.

We have in mind inventing the circuit in Fig. 4 for performing arithmetic and logic operations.

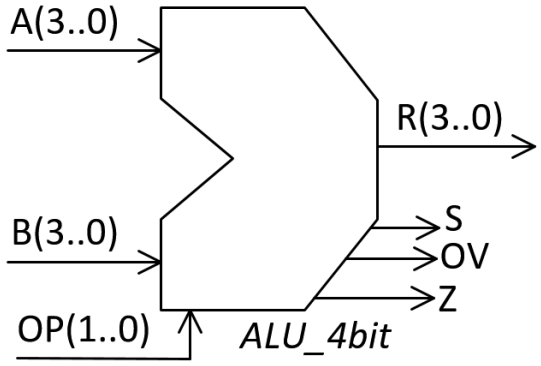


Fig. 4
Symbol and operations performed by the arithmetic and logic unit (ALU_4bit)

OP	Function	
00	A + B	Arithmetic (4-bit signed integer in two's complement)
01	A – B	Arithmetic (4-bit signed integer in two's complement)
10	A · B	Logic AND
11	A ⊕ B	Logic XOR

a) Deduce some examples of the circuit's truth table solving the four operations for the following data (12 stimulus). Express inputs and outputs in the right radix and indicate *don't care* ('x') results when necessary. (0.5p)

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A = "0101"      B = "1010"
A = "1111"      B = "1001"
A = "1000"      B = "1000"
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OP	A	B	R	S	OV	Z

b) Propose an internal architecture for this *ALU_4bit* circuit based on plan C2. Use as a component a 4-channel quadruple multiplexer (Quad_MUX_4) and other blocks and logic gates if necessary. Determine how many VHDL file contain your architecture. (1p)

c) Design flag indicators S, OV and Z using logic gates. (0.5p)

d) Invent the XOR block using only NOR. (0.5p)