## Problem 1

a) $Y = \prod_4 M(8, 12)$

$W = \sum_4 m(1, 2, 5, 6, 14, 15)$

$W(D, C, B, A) = D'C'B'A + D'C'BA' + D'CB'A + D'CBA' +$

$+ DCBA' + DCBA$

$W(1, 0, 1, 1) = 1'0'1'1 + 1'0'11' + 1'01'1 + 1'011' +$

$+ 1011' + 1011 = 0 + 0 + 0 + 0 +$

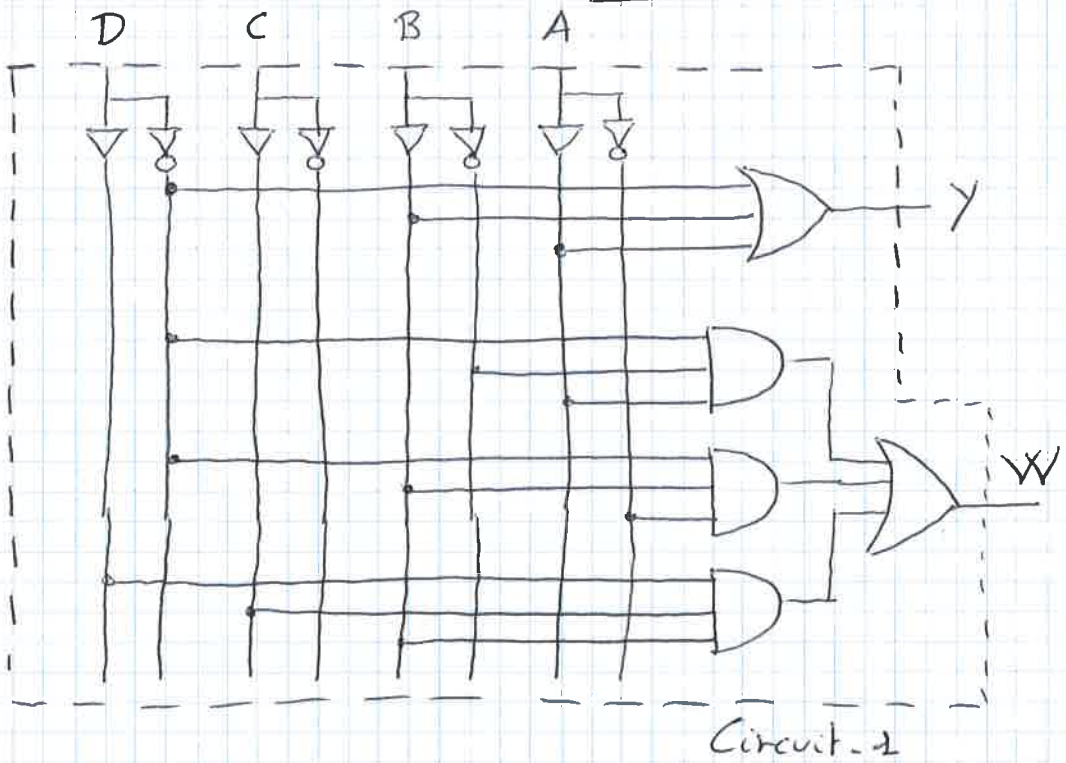
$+ 0 + 0 = \boxed{0}$

b) $Y = D' + B + A$

$W = D' \cdot B'A + D'BA' + DCB$

$W(1, 0, 1, 1) = 1' \cdot 1' \cdot 1 + 1'11' + 1 \cdot 0 \cdot 1 = \boxed{0}$

$Y(1, 0, 1, 1) = 1' + 1 + 1 = \boxed{1}$




Circuit 1

c)

```
Entity Circuit_1 is
        port (
                D, C, B, A : in std_logic;
                Y, W : out std_logic
              );
end Circuit_1;

Architecture equacions of Circuit_1 is
Begin
    Y <= Not (D) OR (B) OR (A).
    W <= Not(D) AND Not(B) AND (A) OR
         Not (D) AND (B) AND Not (A) OR
          D AND C AND B;
end equacions;
```

d)

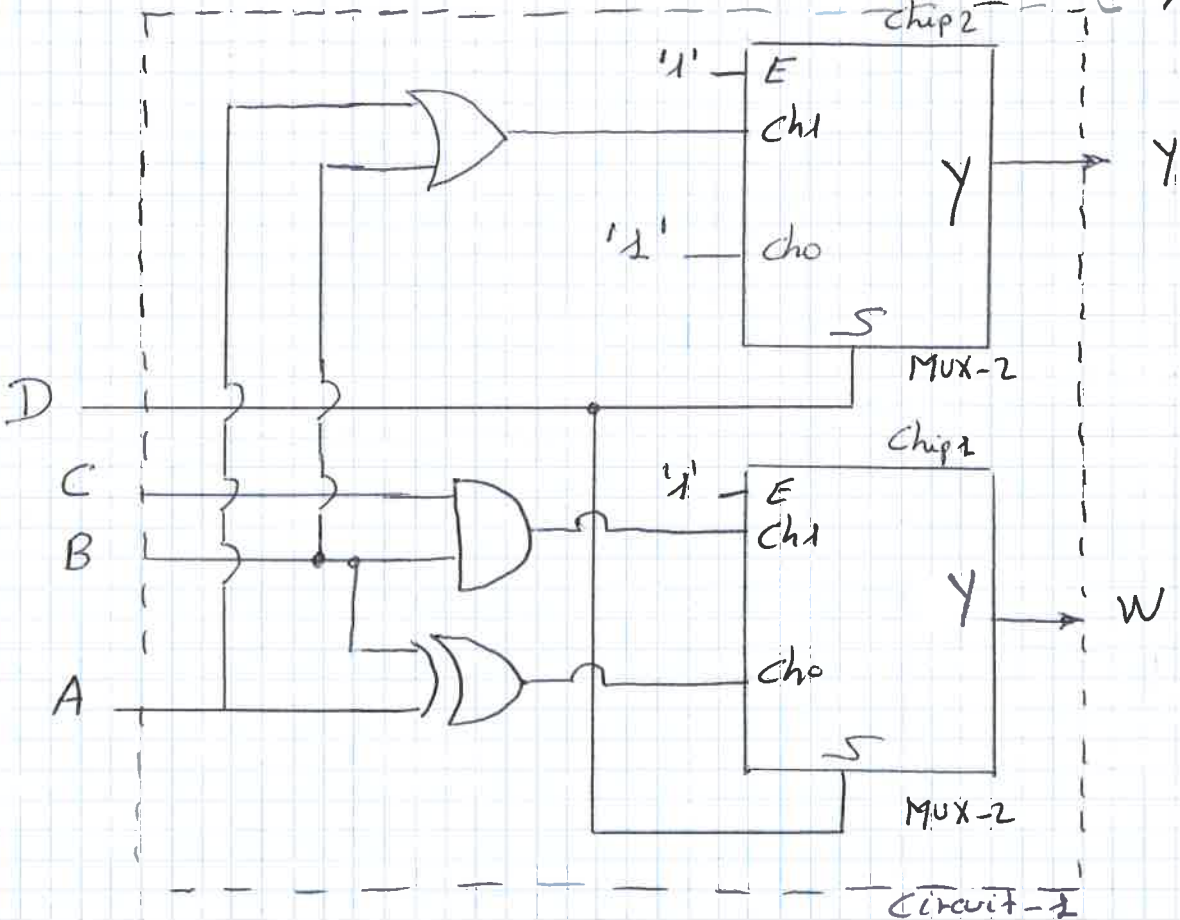
| D | C | B | A | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

C BORA

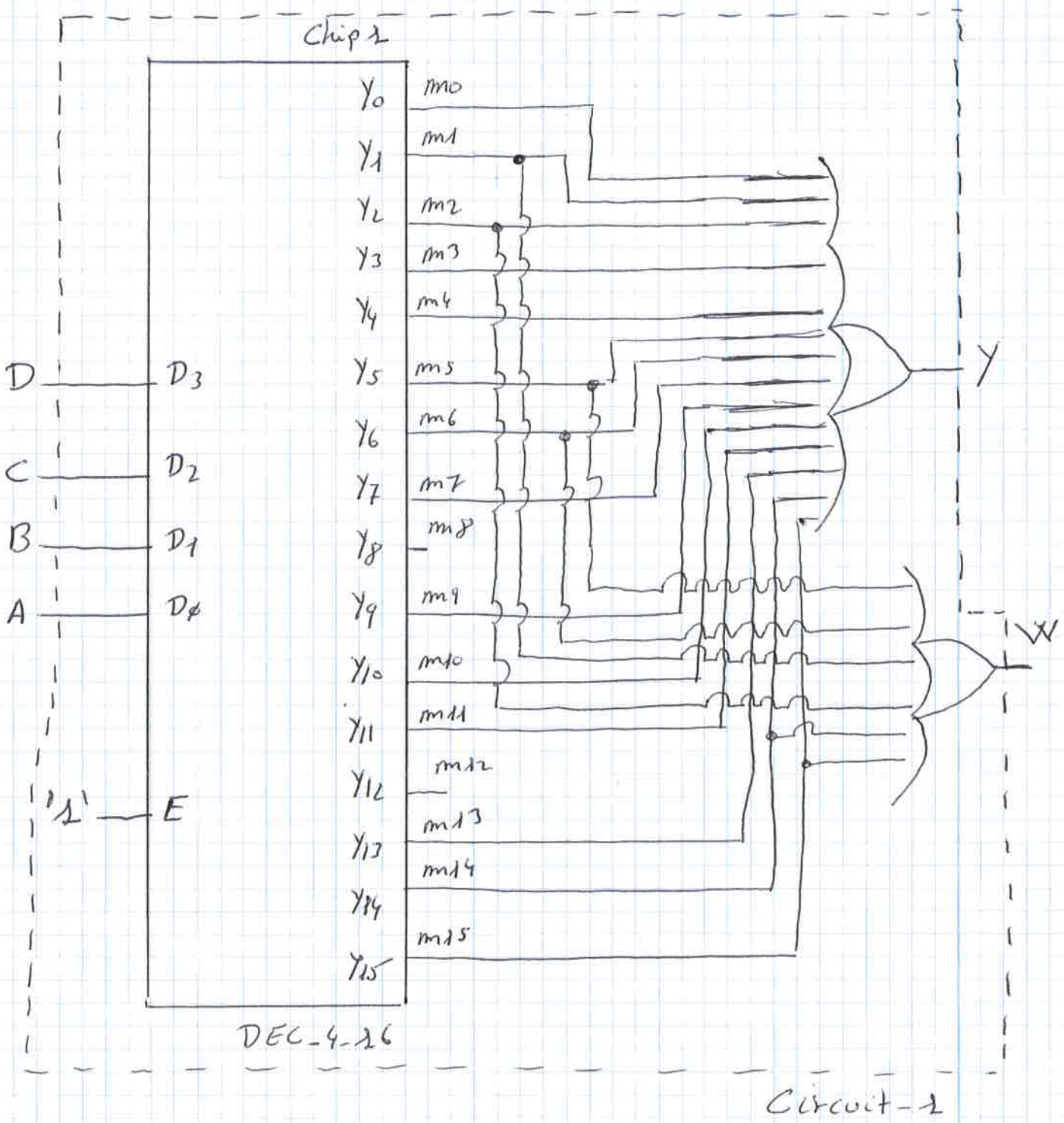
| D | C | B | A | W |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

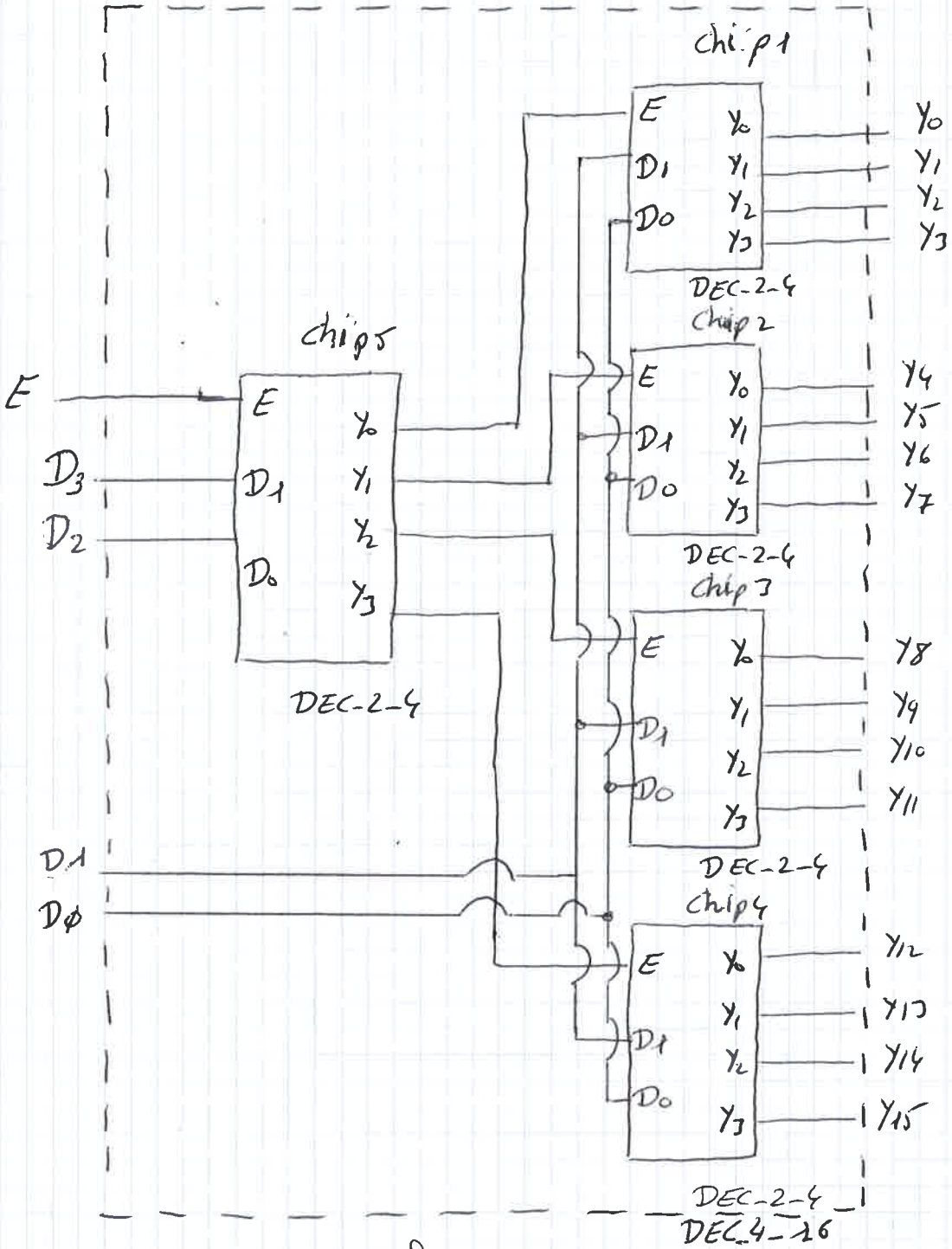
B XOR A

C AND B



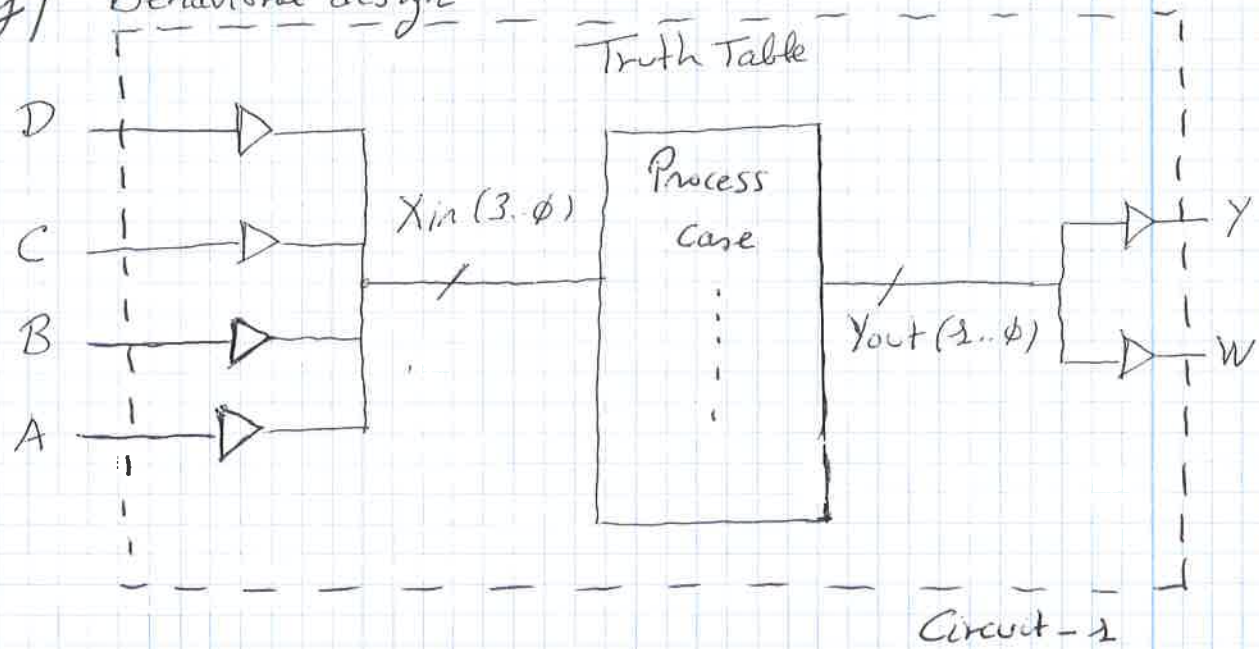
e)


Chip 1
D
C
B
A
'1'
D3
D2
D1
D0
E
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Y10
Y11
Y12
Y13
Y14
Y15
m0
m1
m2
m3
m4
m5
m6
m7
m8
m9
m10
m11
m12
m13
m14
m15
Y
W
DEC_4_16
Circuit_1




3 VHDL files are required : The top file (Circuit_1) and the DEC-2-4 VHDL file and the DEC_4_16

1) Behavioral design




```
Entity Circuit_1 is
        port (
                D, C, B, A : in std_logic;
                Y, W : out std_logic
              )
end Circuit_1;

Architecture truth_table of Circuit_1 is
 Signal Y_out : std_logic_vector (1 downto 0);
 Signal X_in : std_logic_vector (1 downto 0);

Begin
      Process ( X_in )
            Begin
                  Case X_in is

                  When "0000" =>
                        Y_out <= "10";
                  When "0001" =>
                        Yout <= "11";
                  : : : : :
                  When "1110" =>
                        Y_out <= "11";
                  When others =>
                        Yout <= "11";
      END PROCESS;
```

```
Y <= Y_out(1);
W <= Y_out(0);
X_in(3) <= D;
X_in(2) <= C;
X_in(1) <= B;
X_in(0) <= A;
end truth_table;
```