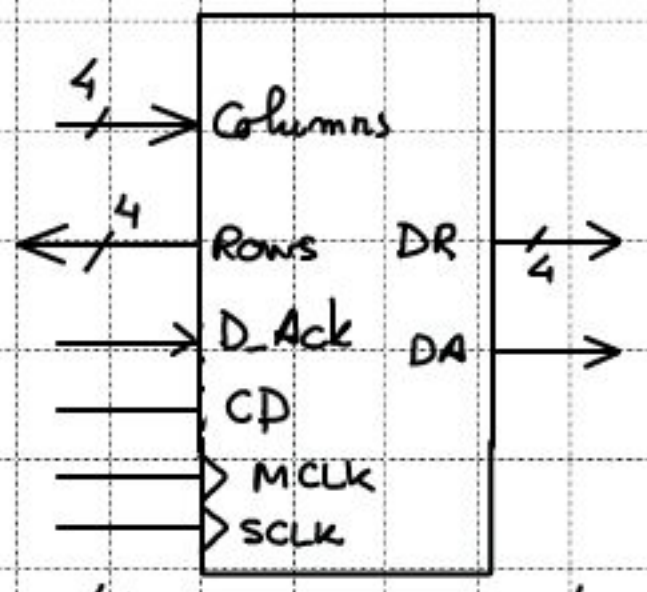
The problem of interfacing the keyboard encoder

PG - Part 2



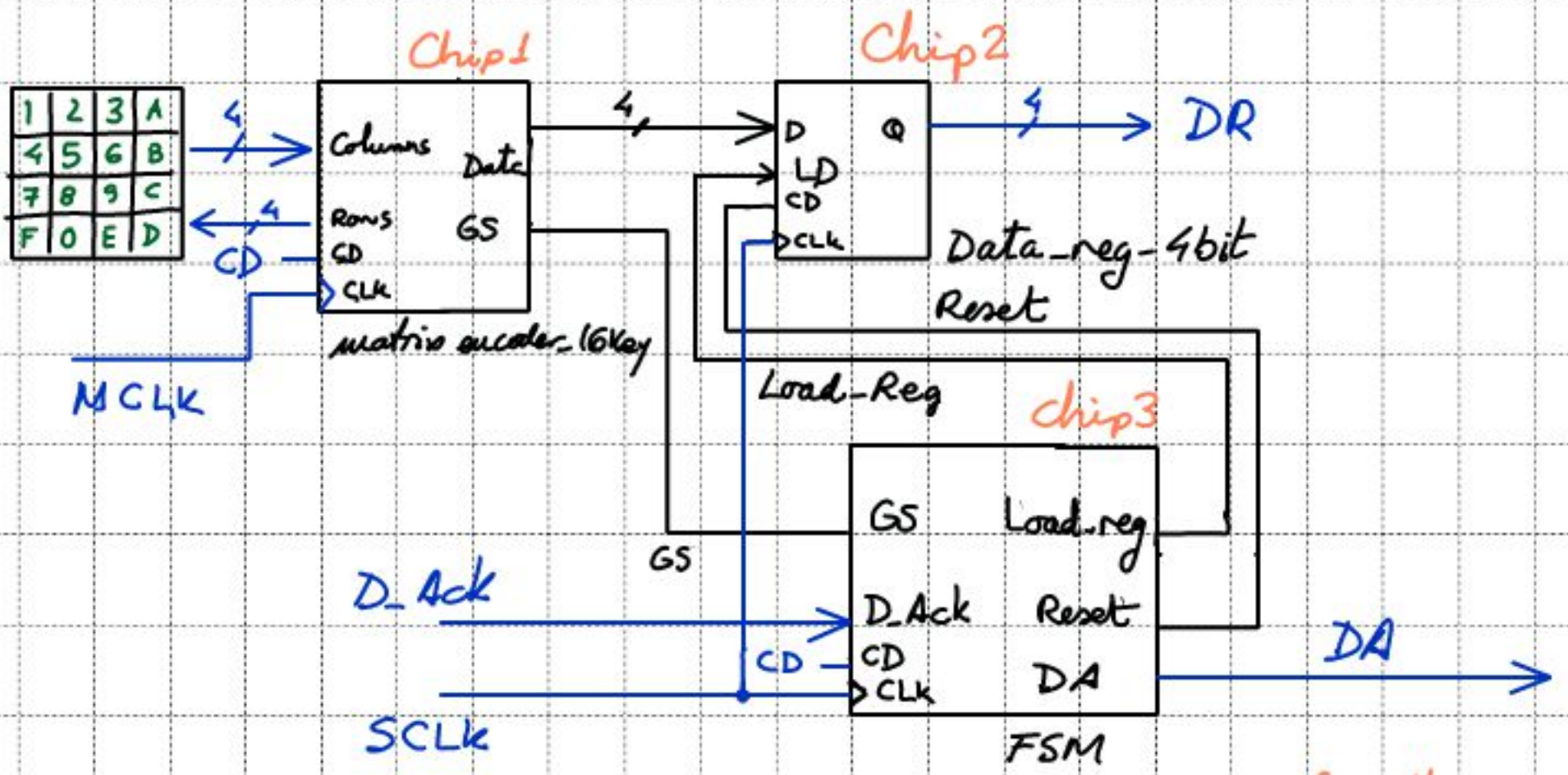
matrix_encoder_16key_registred

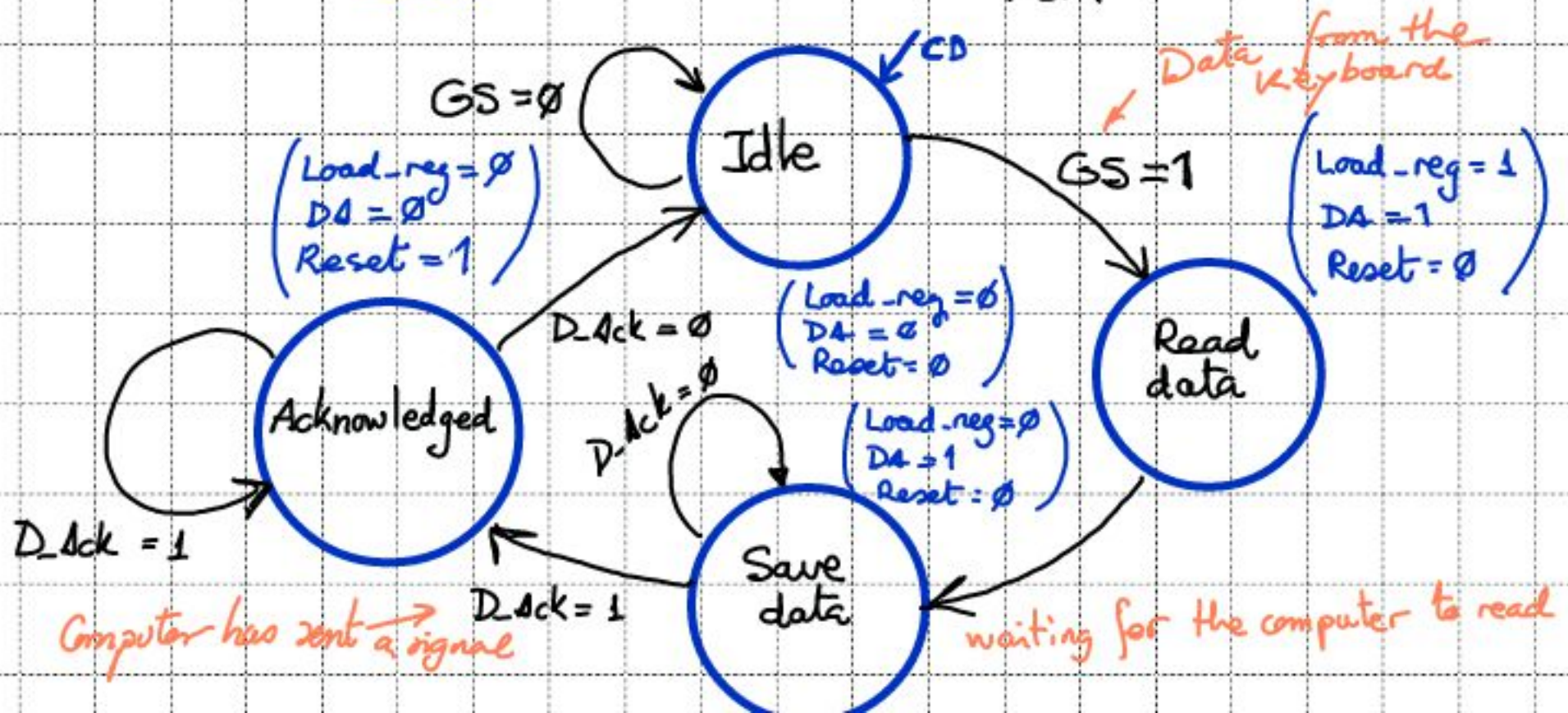
200 kHz → MCLK, 100 kHz → SCLK

- 2 CLK : MCLK , SCLK
- Peripheral to be under the control of master device (control unit, microcontroller, etc)

{ DA : data available flag
D_Ack : data acknowledged
DR : registered data that cannot be erased until the master device has read it.

⇒ DR and DA must be synchronous with the system clock (SCLK)





This is an example of timing diagram

SCLK

CD

Key released

Key pressed

Key released

Data

0 9 0 D 0

GS

1 1

Key pressed (synchronous with the MCLK)

D_Ack

1 1 1

Load_Reg

1 1

Reset

DA

DR

0 9 0 D 0

The controller reads now the saved data

current_state

Idle | Saved data | Idle | Idle

Read Data

Acknowledged

Read Data

Acknowledged

Saved data

D_Ack may take longer than a single synchronous SCLK. This is why it can be in 'Saved data' several SCLK's