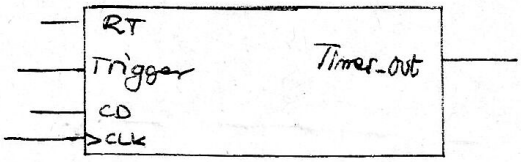
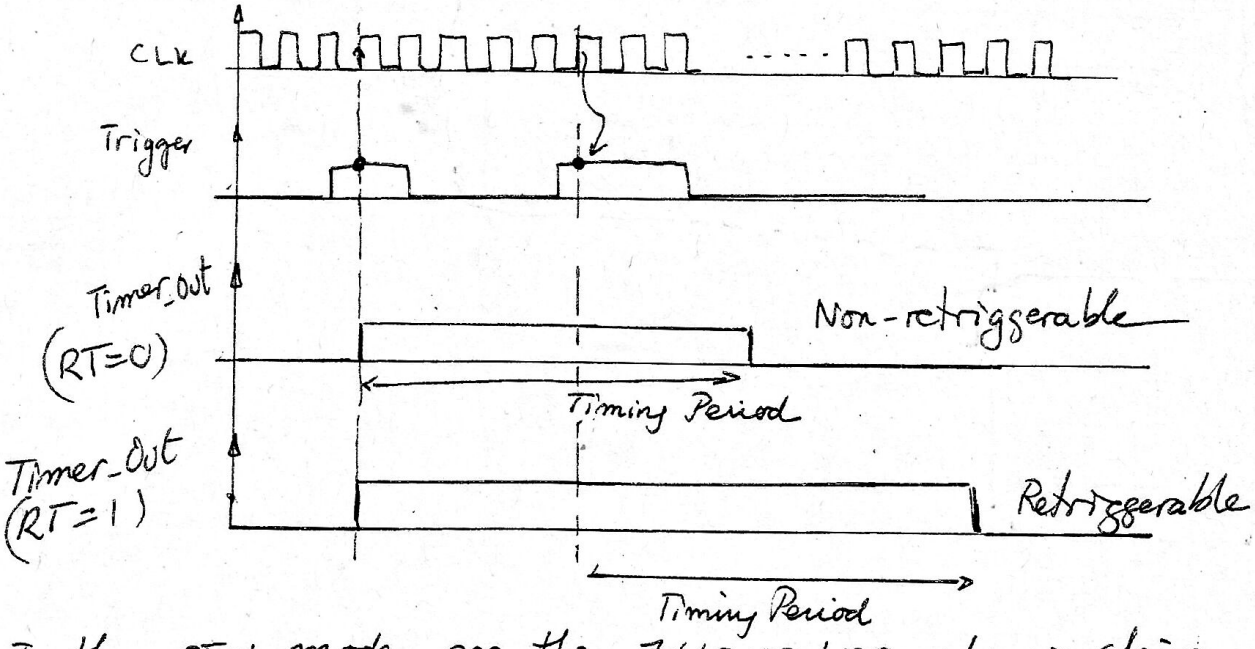
Designing a Timer

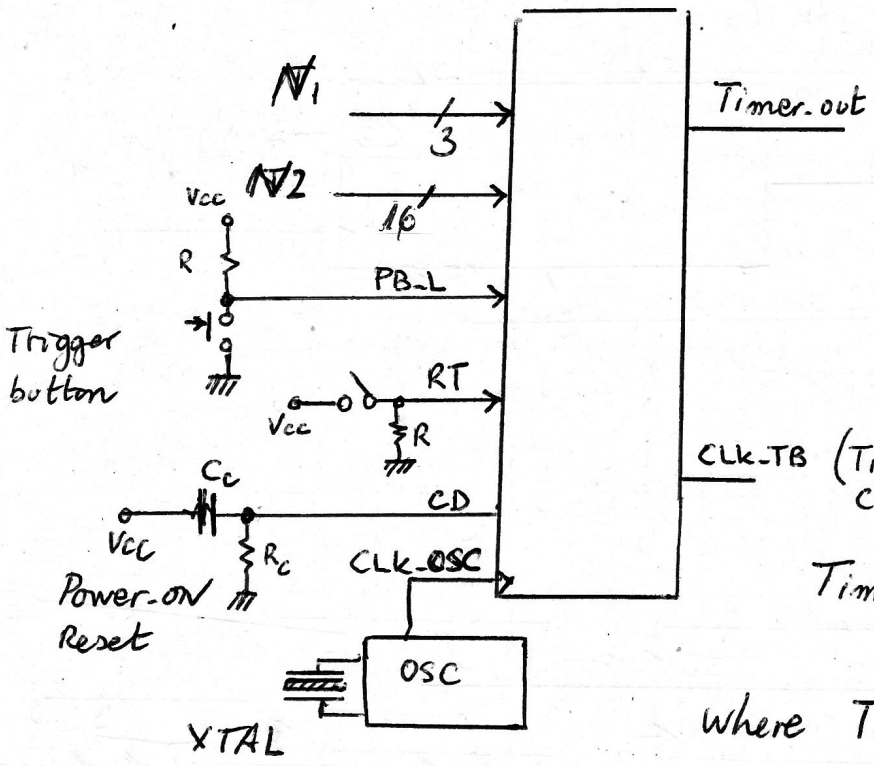


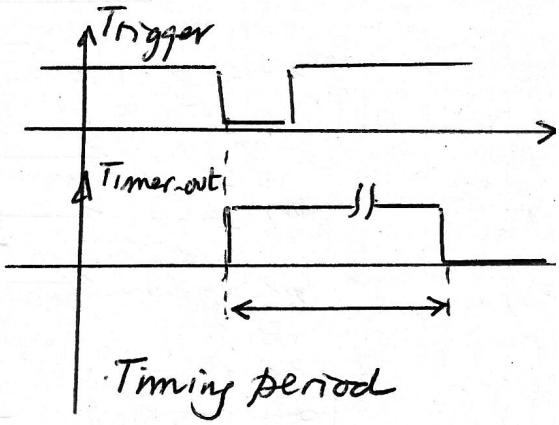


- In the RT=1 mode, see the 74LS122/123 classic chip, the timing period can be extended as desired because the timing period starts again every time that a Trigger signal is detected. This is the functionality of a "watch-dog" timer.
- A non-retriggerable timer do not consider other trigger pulses while timing, so that always a fixed timer period is generated. (see the classic chip 74LS121)

→ Let's try first, to approach the design using concepts from previous chapters

Idea of a programmable timer





$$\text{Timing period} = T_{CLK\_TB} \cdot N_1 \cdot N_2$$

where $T_{CLK\_TB} = T_{CLK\_OSC} \cdot M$

The period of the time base (CLK_TB) is generated internally by the CLK_Generator circuit and is a multiple (M) of the external oscillator (CLK_OSC)

$N_1 \rightarrow$ will program the prescaler value
$(2, 4, 8, \ldots, 256)$

$N_2 \rightarrow$ will program the counter value
$(1, 2, \ldots, 65535)$ ← 16 bit

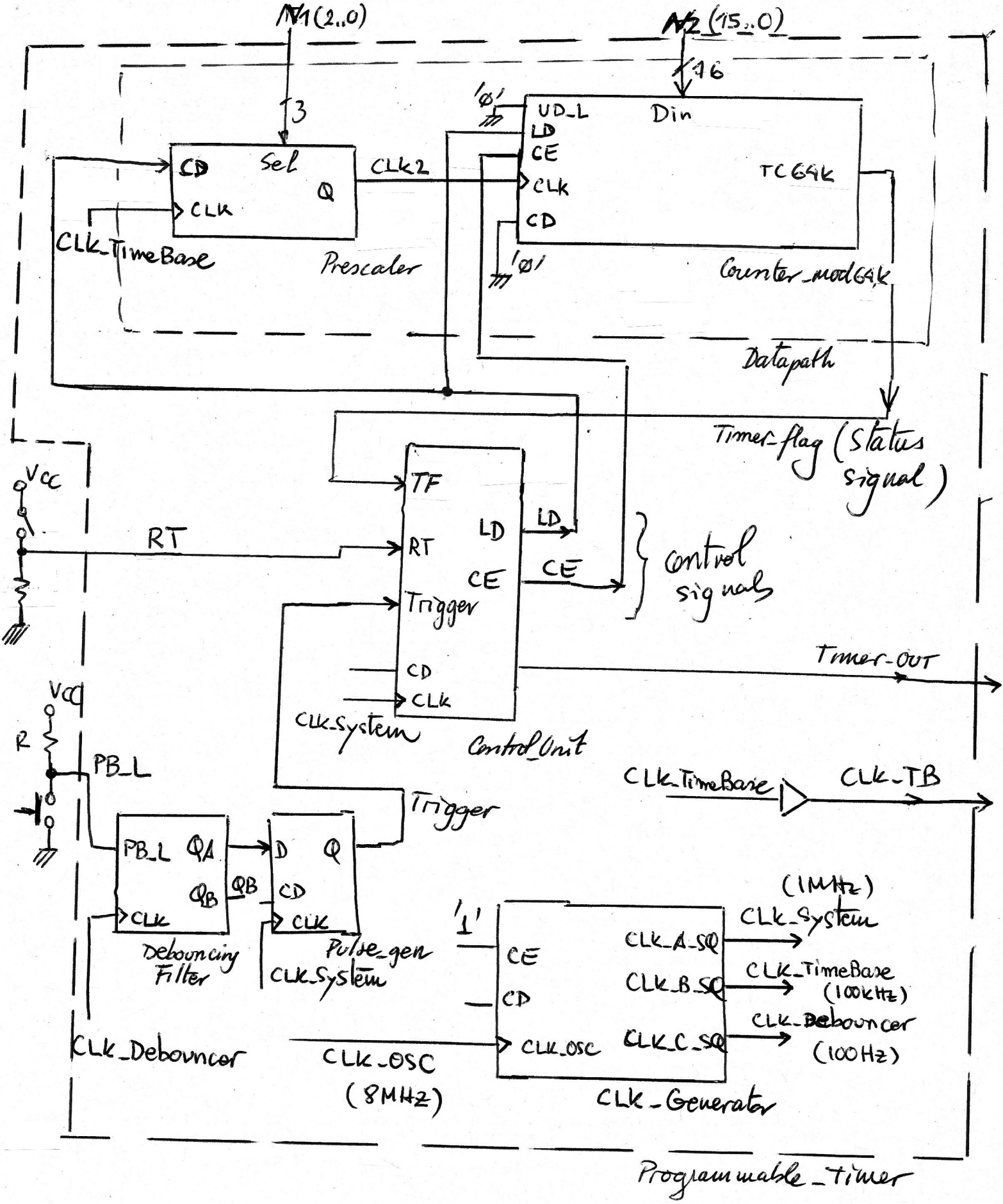
For instance, if XTAL = 8 MHz and $M = 80 \Rightarrow T_{CLK\_TB} = 10\,\mu s$ (100 kHz)

if $N_1 = 32$, $N_2 = 125$

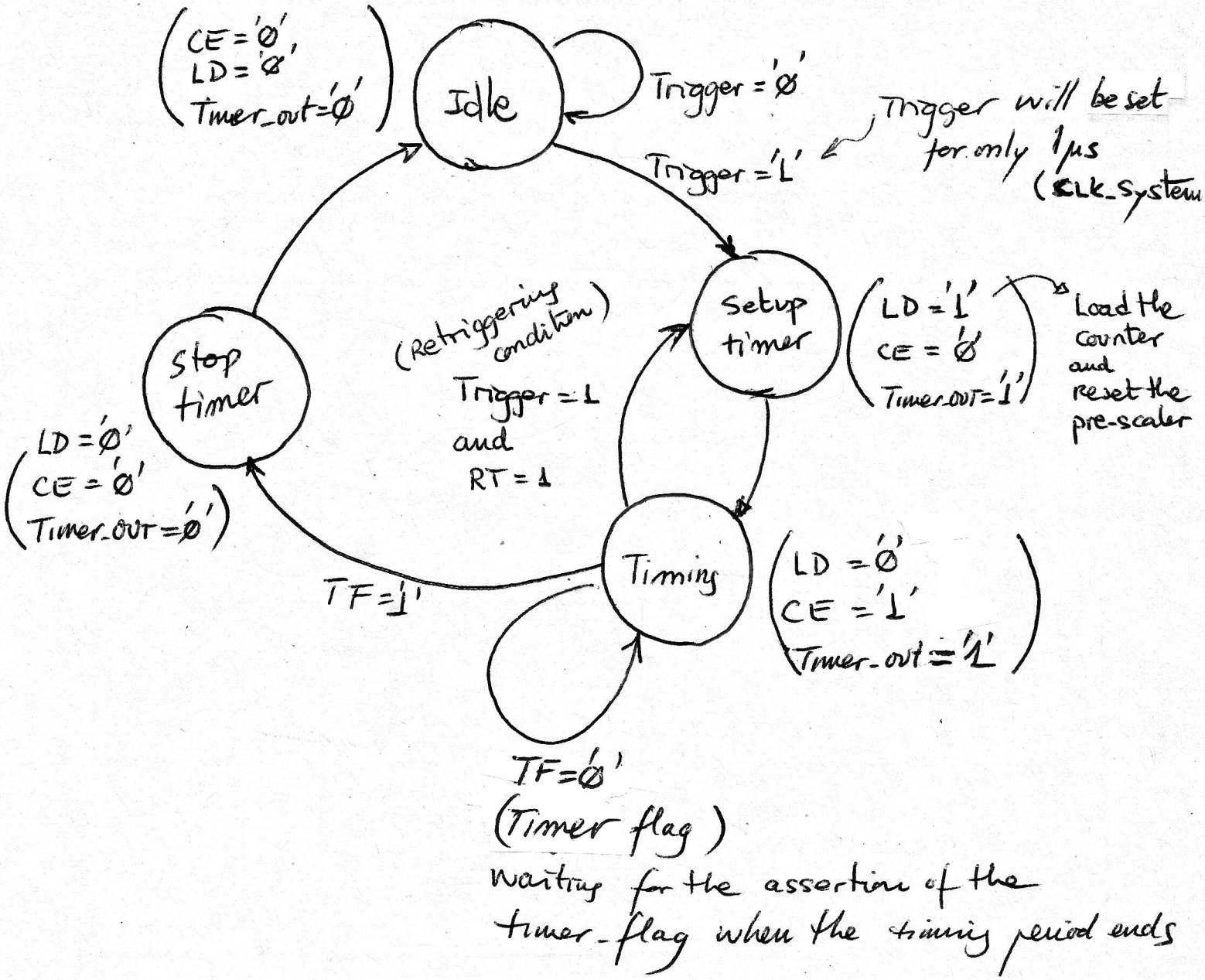
Timing period = $125\,ns \cdot 80 \cdot 32 \cdot 125 = \underline{40\,ms}$

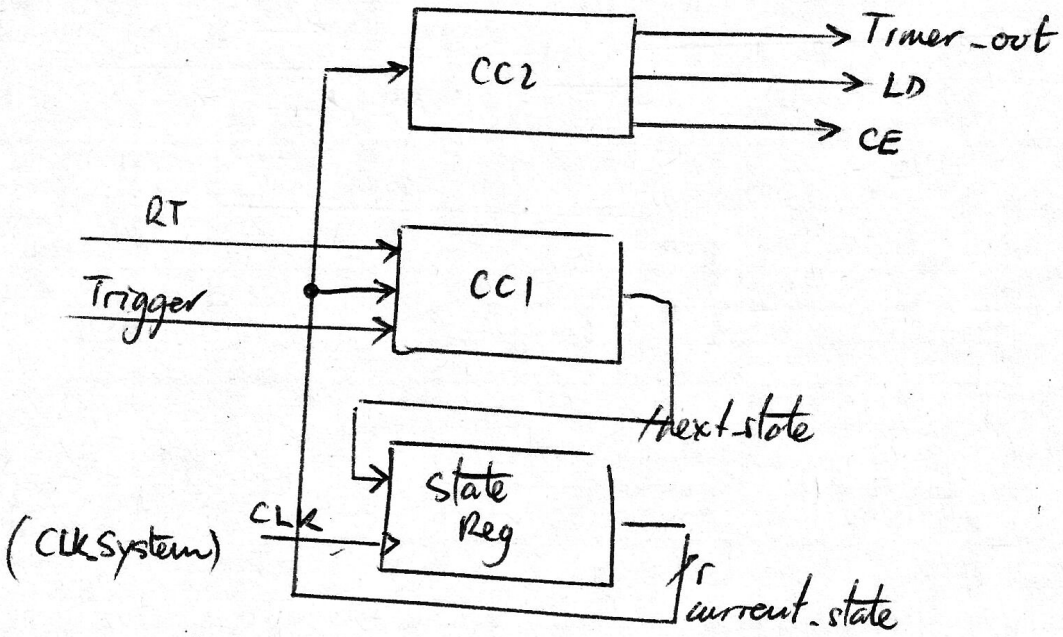
if $N_2 = 3125 \rightarrow$ Timing period = $125\,ns \cdot 80 \cdot 32 \cdot 3125 = \underline{1\,s}$

Example architecture for a programmable timer

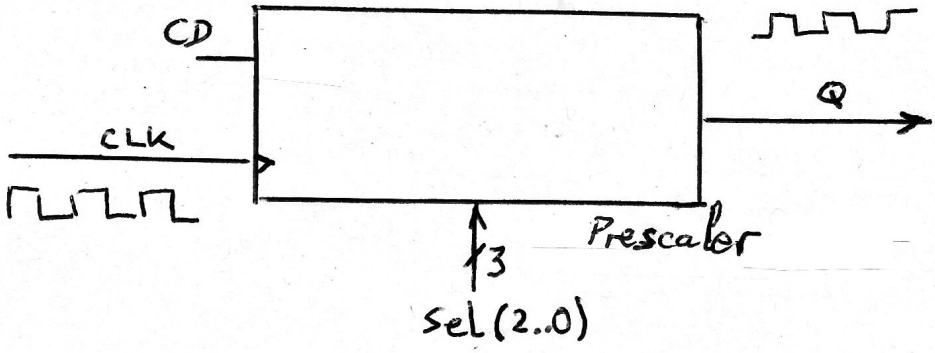


State diagram for the Control Unit



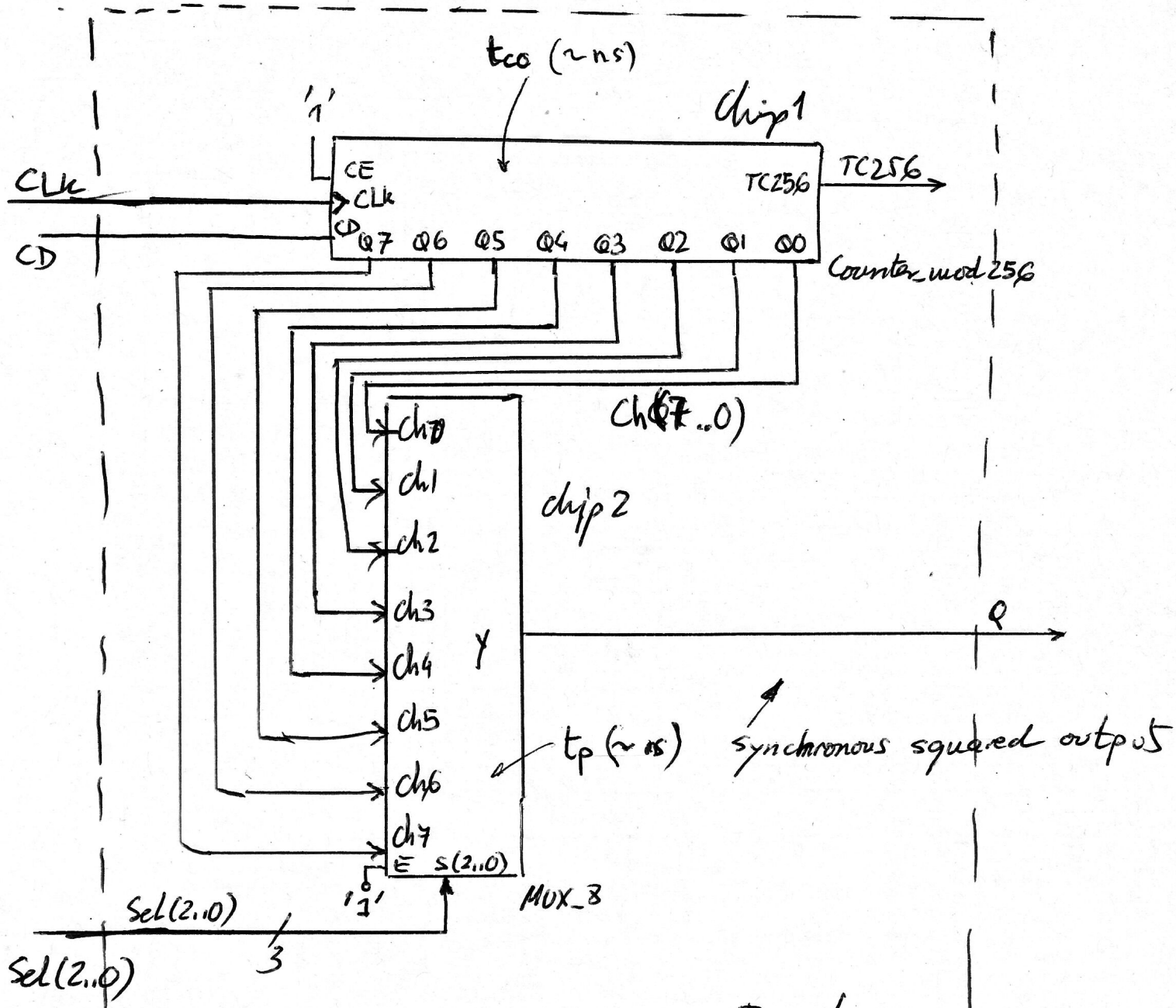


Idea of a programmable synchronous prescaler

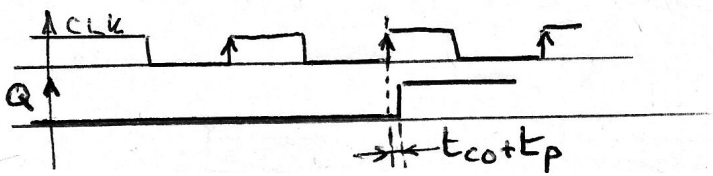


sel	
000	÷ 2
001	÷ 4
010	÷ 8
011	÷ 16
100	÷ 32
101	÷ 64
110	÷ 128
111	÷ 256

A MUX_8 is right to select a given output

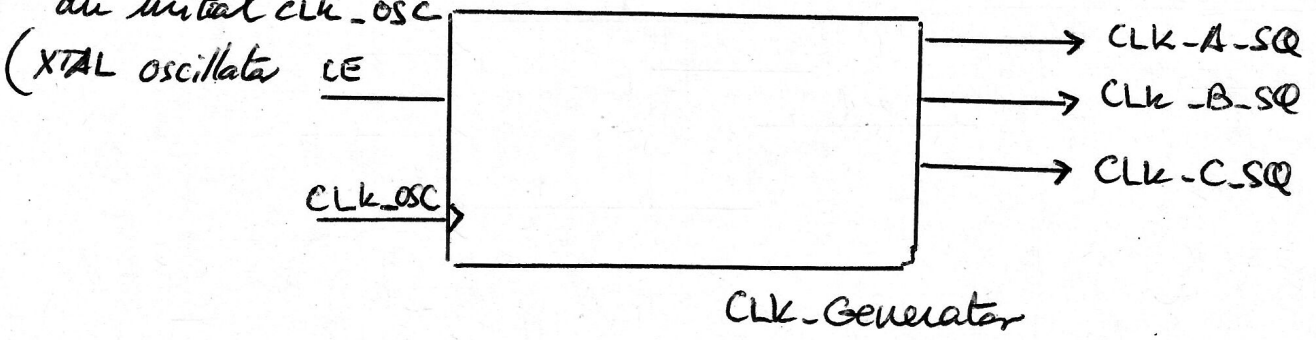


Prescaler

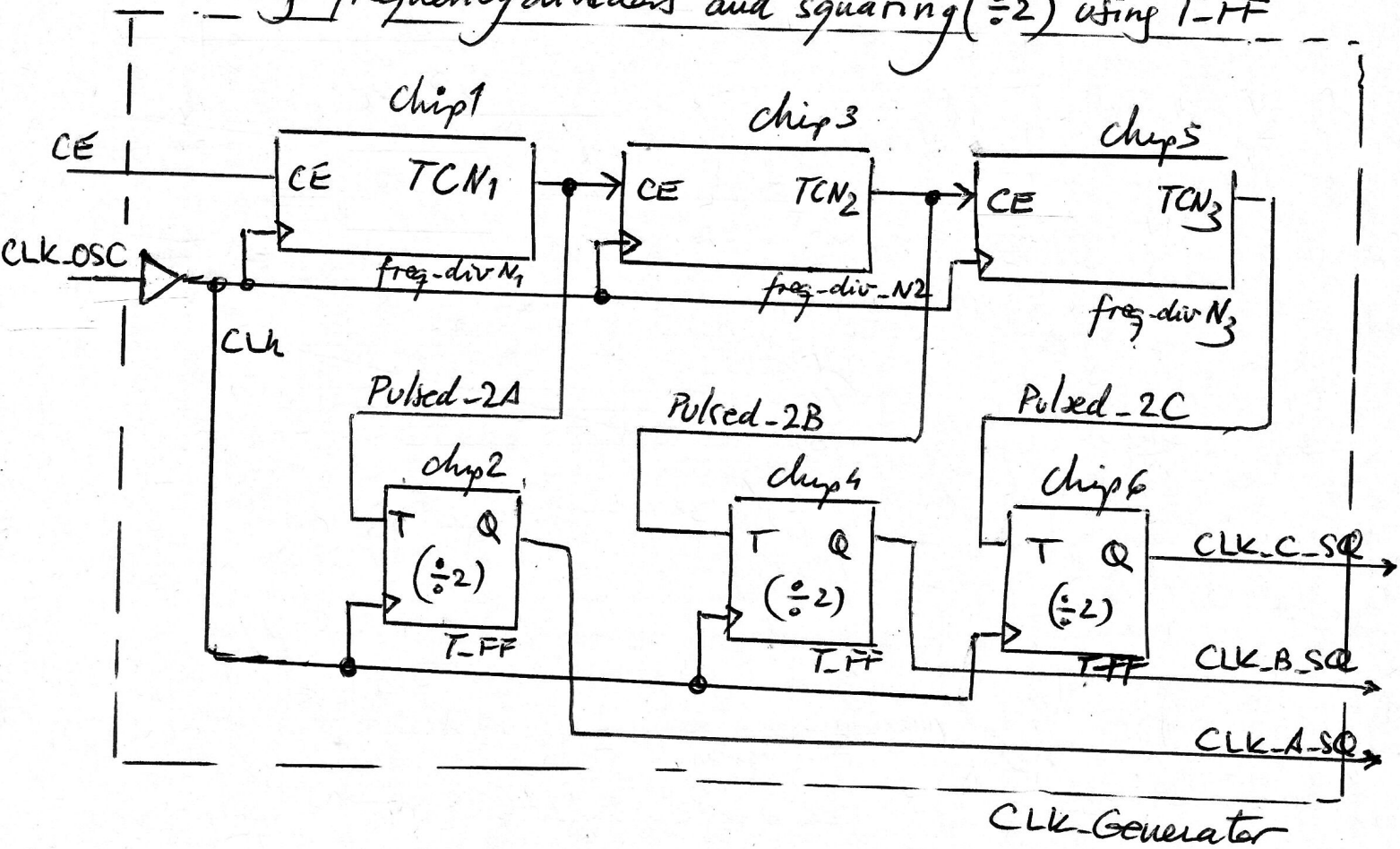


Idea on the design of the CLK_Generator

The concept is obtaining squared and synchronous signals from an initial CLK_OSC (XTAL oscillator)



Chaining frequency dividers and squaring (÷2) using T_FF



For instance:

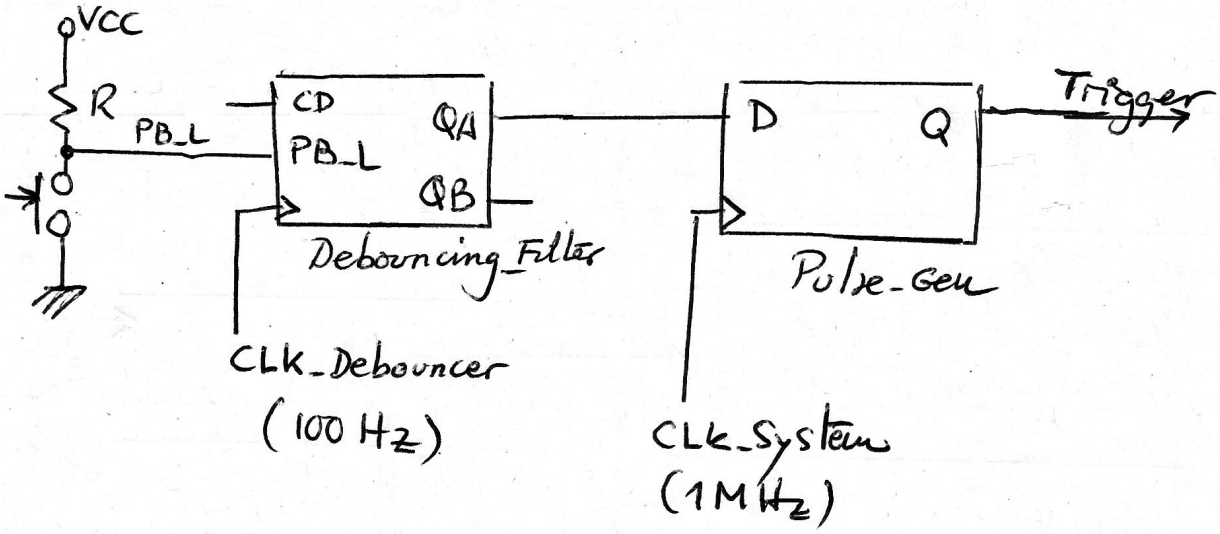
- CLK_OSC → 8MHz
- CLK_ASQ → CLK_System = 1MHz
- CLK_B_SQ → CLK_TB = 100KHz
- CLK_C_SQ → CLK_Debouncer = 100 Hz

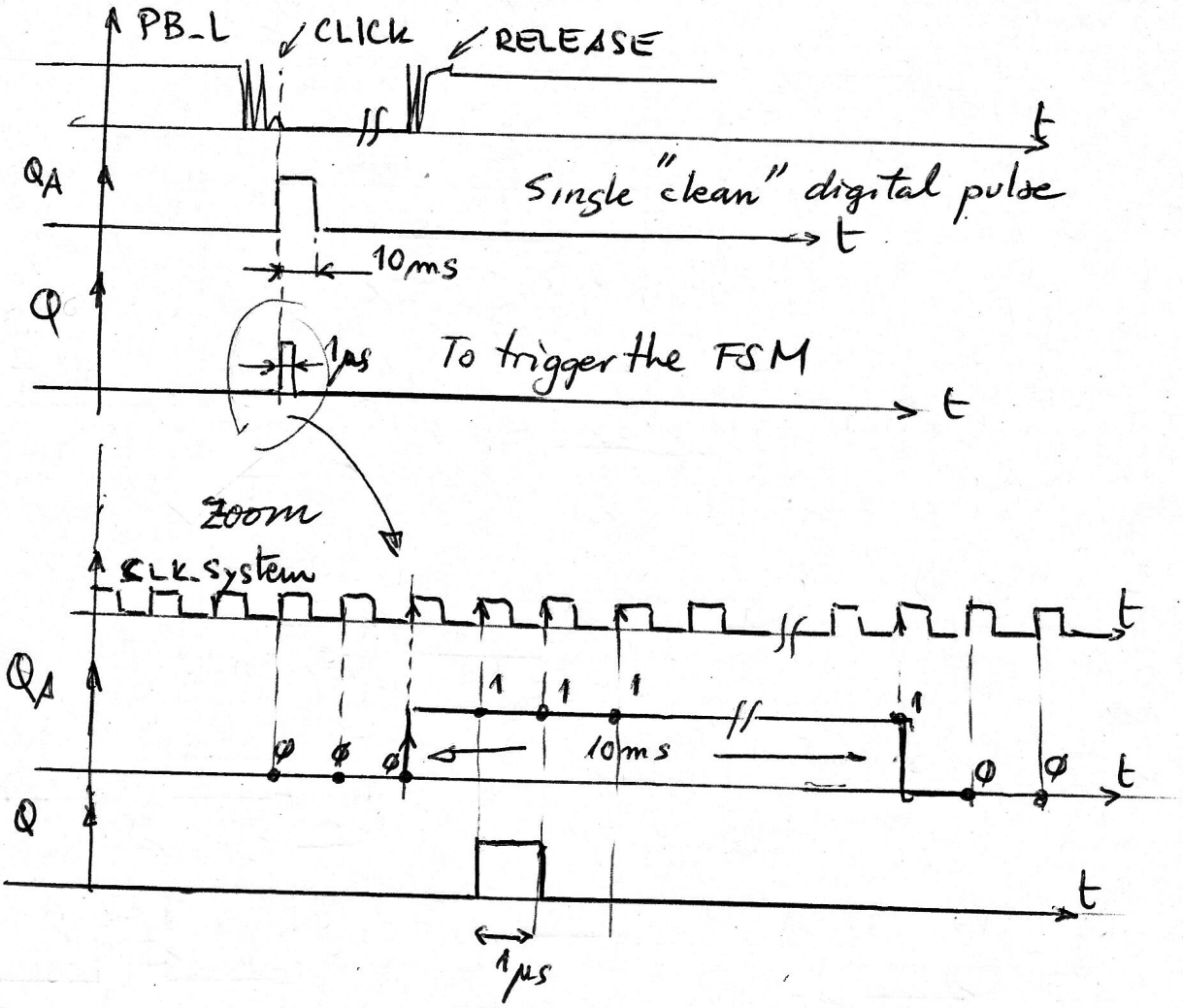
Pulsed 2A → 2MHz → $N_1 = 4$

Pulsed 2B → 200KHz → $N_2 = 10$

Pulsed 2C → 200 Hz → $N_3 = 1000$

Interfacing the trigger button





The CLK_Debouncer frequency (100Hz) is depending of the physical phenomena (Clicking a mechanical button)

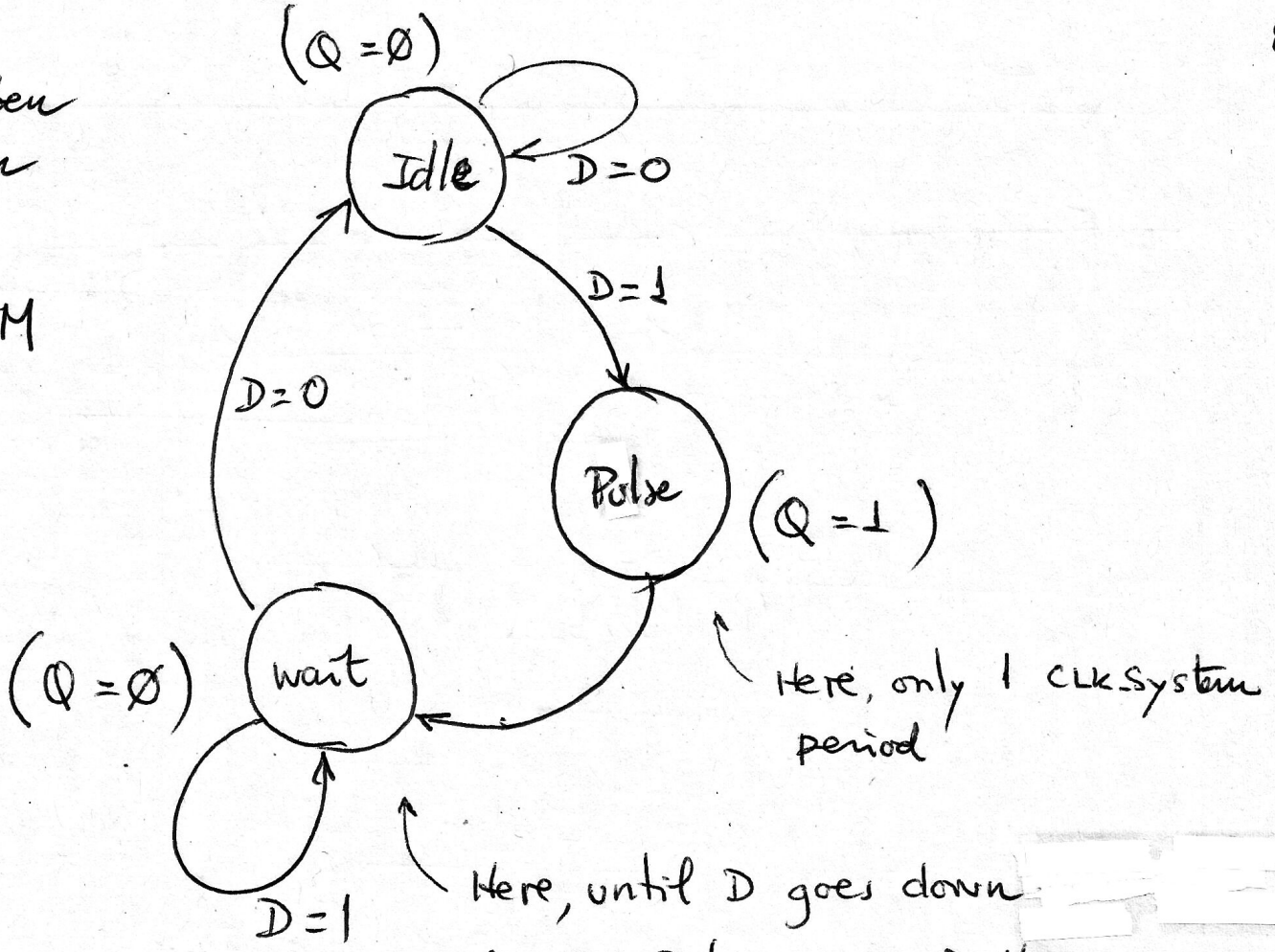
The CLK_system is running the dedicated processor, thus, a synchronous 1μs pulse in Q will trigger the timing operation.

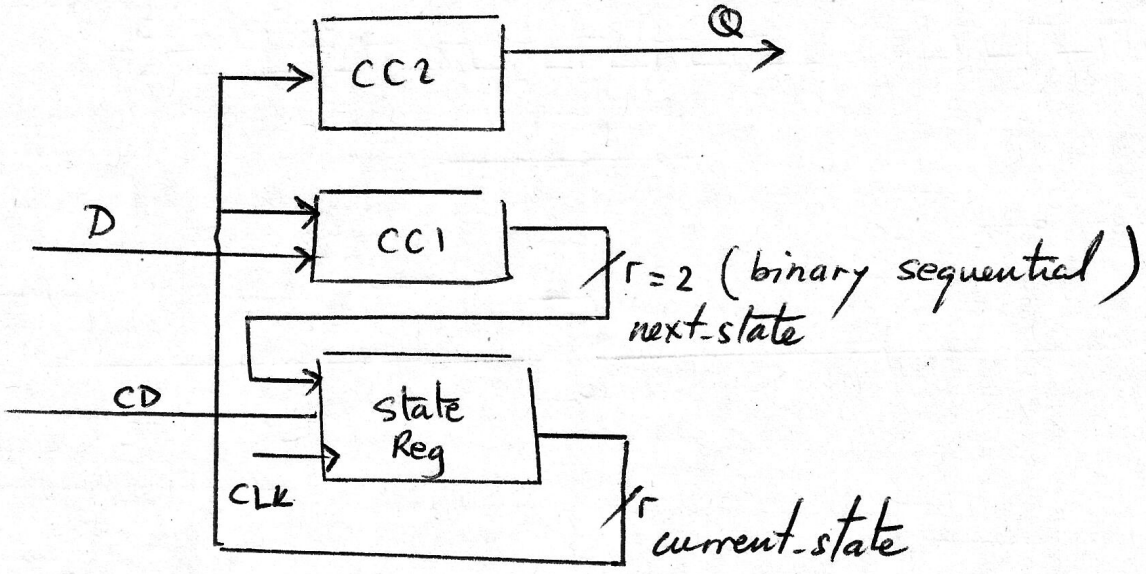
So, the Pulse_Gen circuit is a FSM as follows:

Pulse_Gen design

↓

FSM





current_state	Q
Idle	Ø
Pulse	1
wait	Ø

D	current_state	next_state
Ø	Idle	Idle
1	Idle	Pulse
x	Pulse	Wait
Ø	wait	Idle
1	wait	Wait