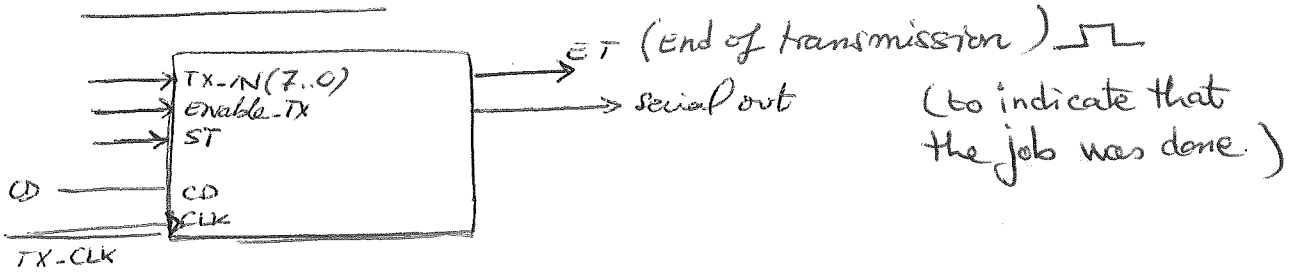
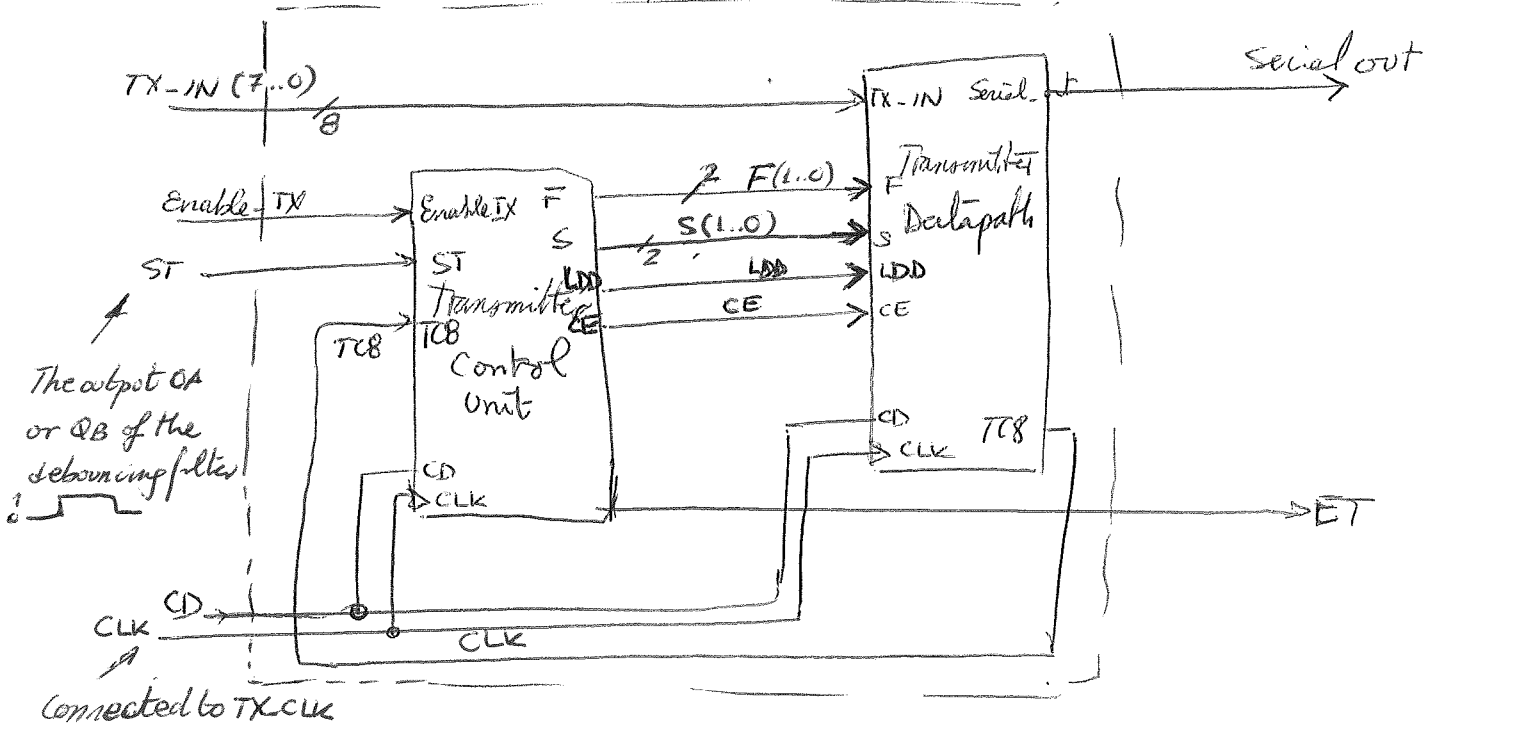
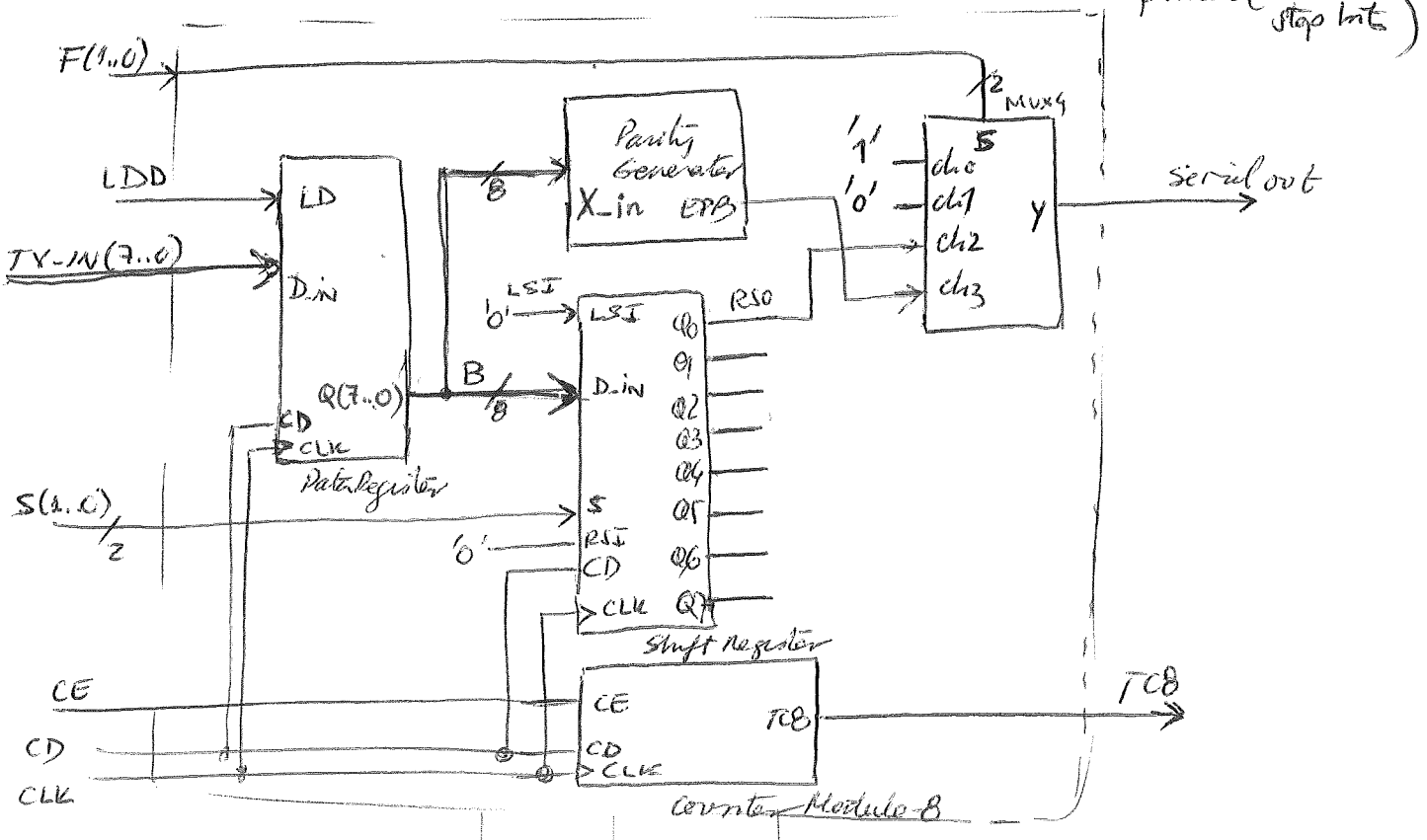
Transmitter Unit .vhd

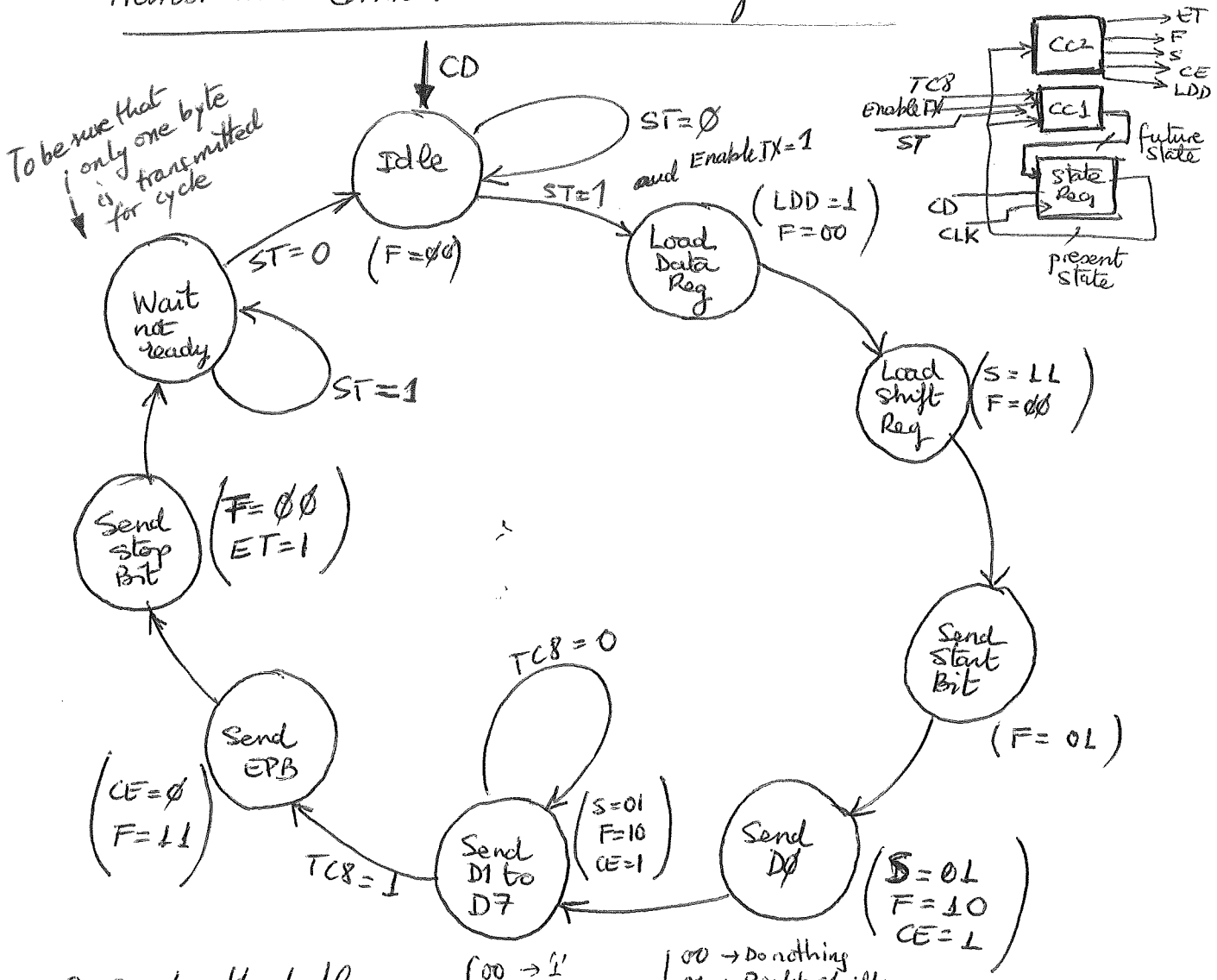




Transmitter_datapath : Resources to store and process data (bit shifting, parity generation, bit counting protocol (start & stop bit)



Transmitter Control Unit state diagram



CC2 truth table

F: 00 → '1', 01 → '0', 10 → RSO, 11 → EPB

S: 00 → Do nothing, 01 → Right shift, 10, 11 → Load data

present state	LDD	F	S	CE	ET
Idle	Ø	ØØ	ØØ	Ø	Ø
Load_Data_Reg	1	Ø Ø	Ø Ø	Ø	Ø
Load_Shift_Reg	Ø	Ø Ø	1 1	Ø	Ø
Send_StartBit	Ø	Ø 1	Ø Ø	Ø	Ø
Send_DØ	Ø	1Ø	Ø 1	1	Ø
Send_D1_to_D7	Ø	1 Ø	Ø 1	1	Ø
Send_EPB	Ø	1 1	Ø Ø	Ø	Ø
Send_Stop_Bit	Ø	Ø Ø	Ø Ø	Ø	1
Wait_not_ready	Ø	Ø Ø	Ø Ø	Ø	Ø

At each state every output has to be set at a given value.

And now invent a timing diagram to figure out how the signals are going to be