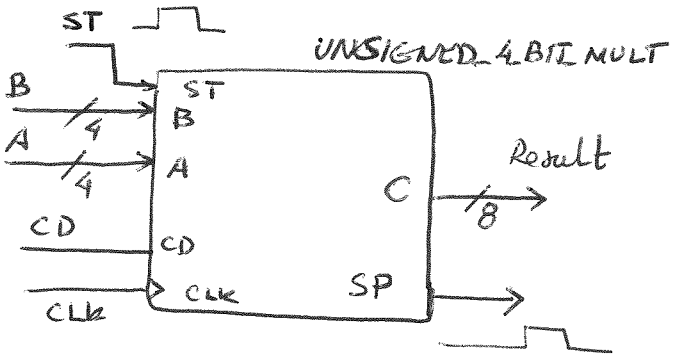
The 4x4 multiplier



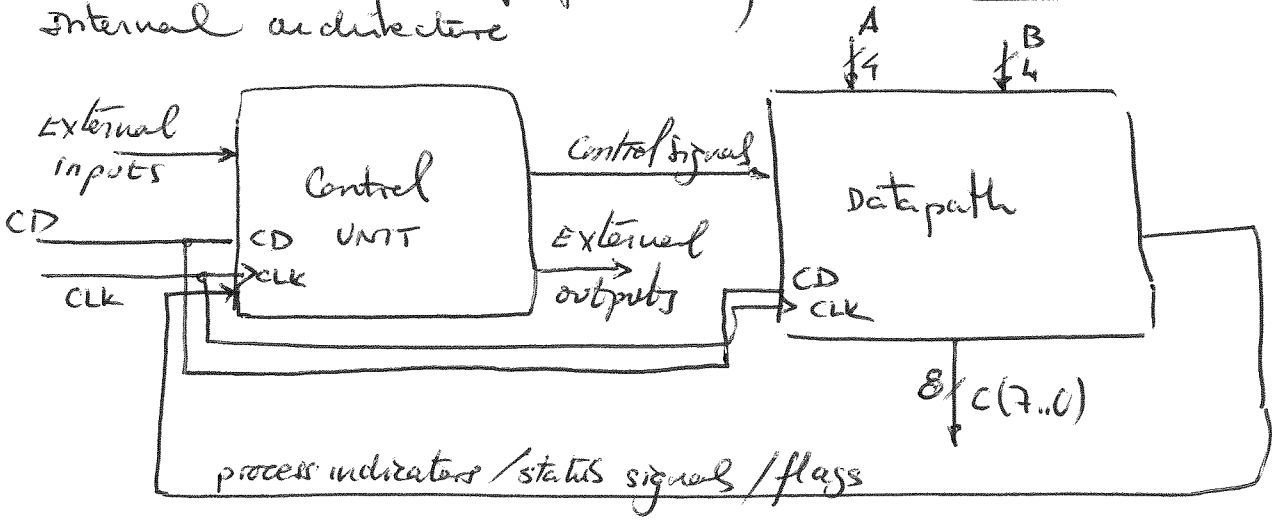
multiplier
multiplicand

A	1 1 0 0	12
x B	x 1 0 1 1	x 11
C	1 1 0 0	
	1 1 0 0	
	0 0 0 0	
	1 1 0 0	
	1 0 0 0 0 1 0 0	132

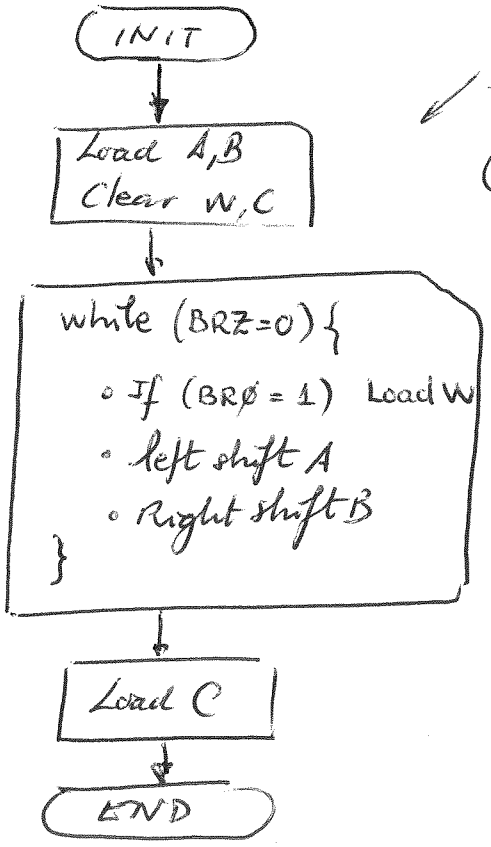
shift + add algorithm

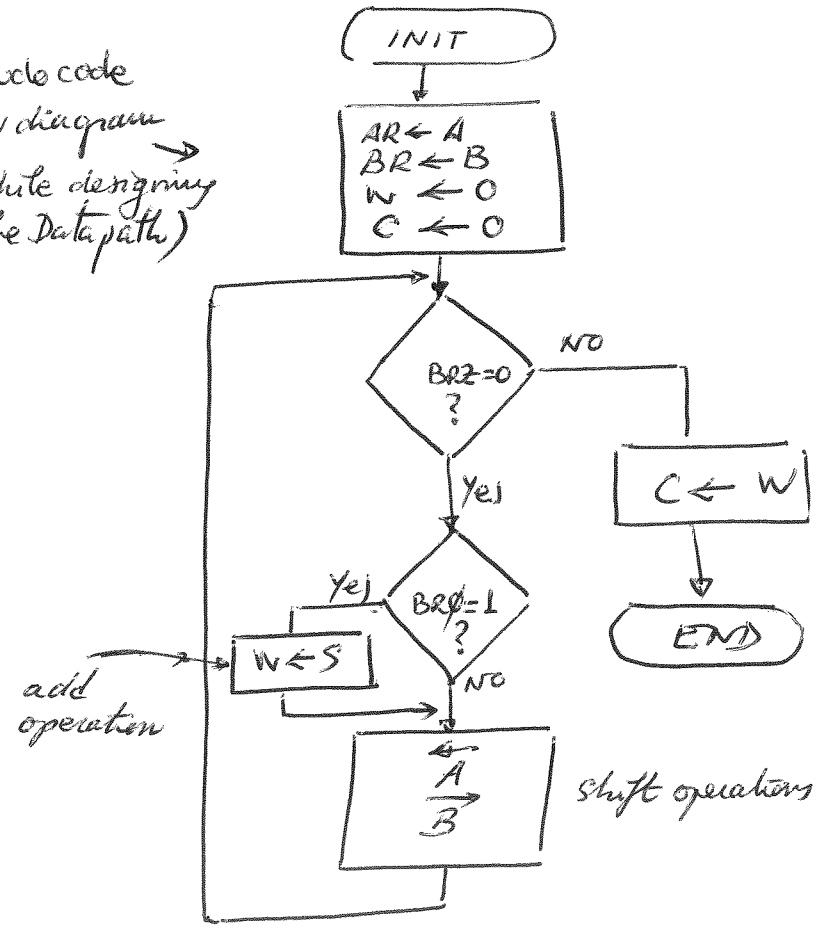
start → ST (start operation)
stop → SP (end of operation)

→ Internal architecture

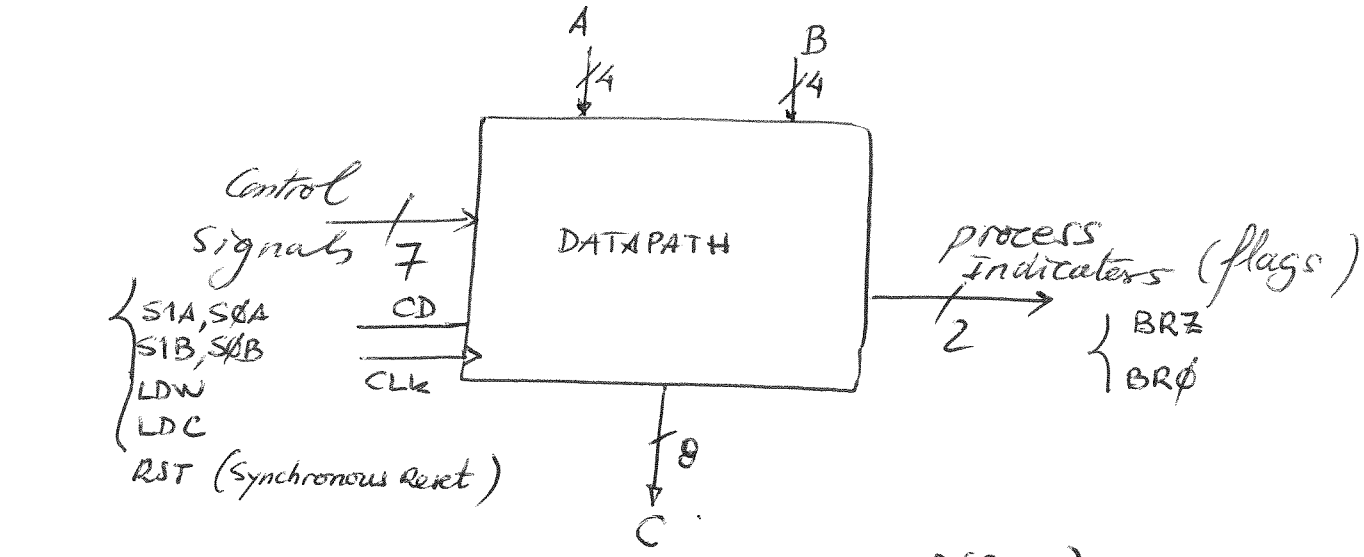


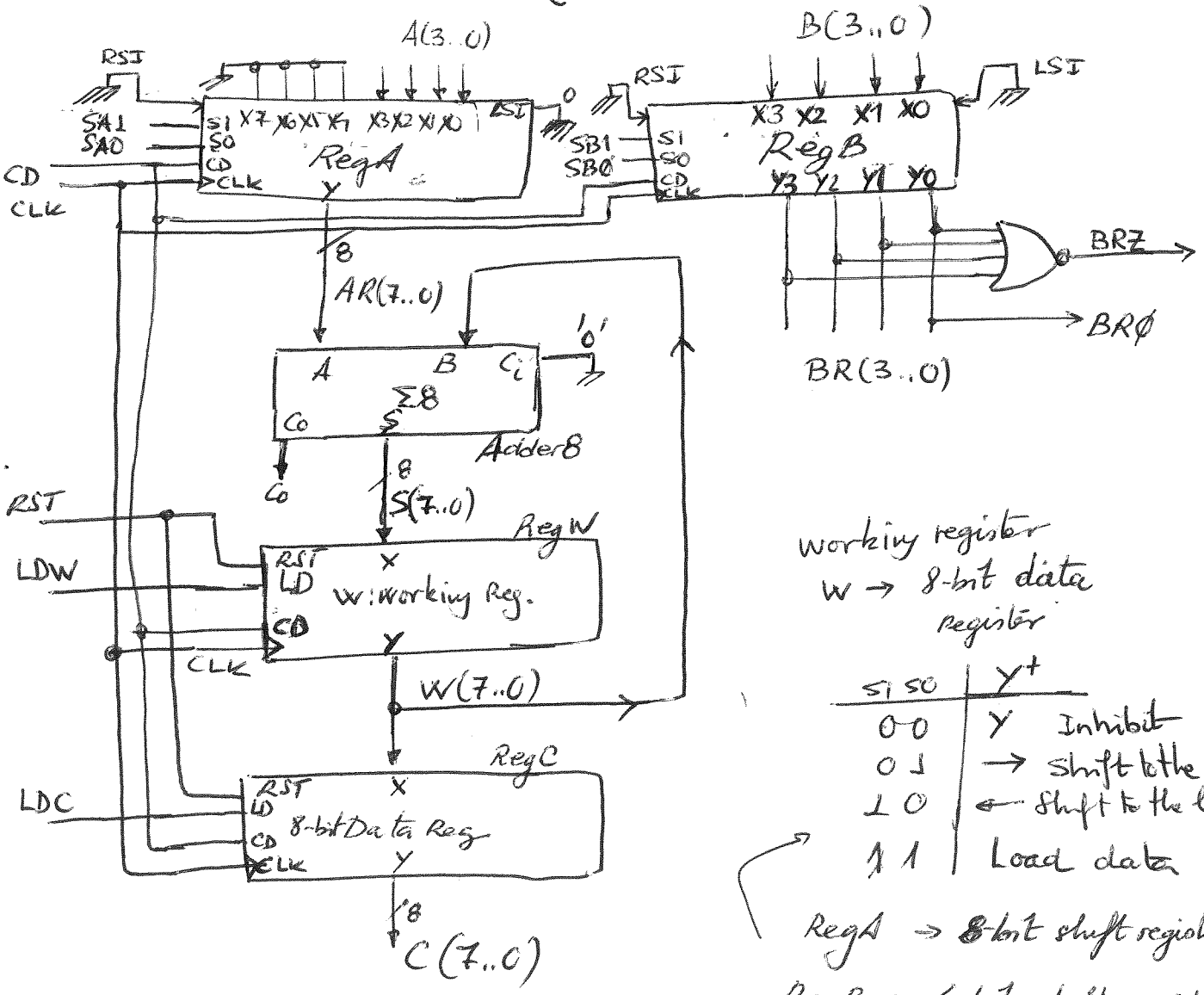
Pseudo code
Flow diagram
(while designing the Datapath)





The datapath or operational unit





Working register
W → 8-bit data register

S1 S0	Y+	
0 0	Y	Inhibit
0 1	→	shift to the right
1 0	←	shift to the left
1 1		Load data

RegA → 8-bit shift register

RegB → 4-bit shift register

RegW, RegC → 8-bit data register