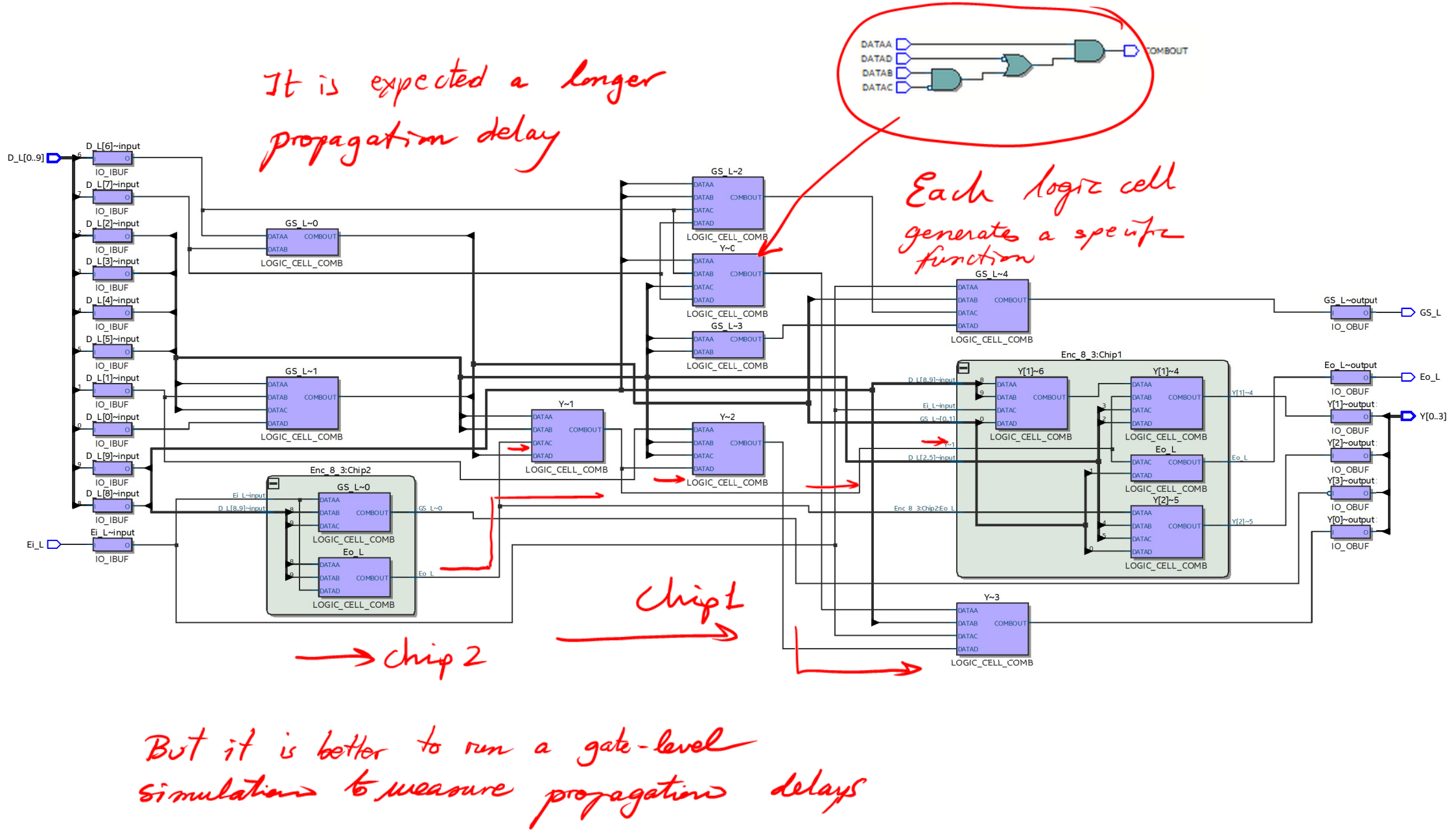
It is expected a longer propagation delay
Each logic cell generate a specific function
DATAA
DATAD
DATAB
DATAC
COMBOUT
D_L[0..9]
D_L[6]~input
D_L[7]~input
D_L[2]~input
D_L[3]~input
D_L[4]~input
D_L[5]~input
D_L[1]~input
D_L[0]~input
D_L[9]~input
D_L[8]~input
Ei_L
Ei_L~input
IO_IBUF
GS_L~0
GS_L~1
GS_L~2
GS_L~3
GS_L~4
Y~0
Y~1
Y~2
Y~3
LOGIC_CELL_COMB
Enc_8_3:Chip1
Enc_8_3:Chip2
Y[1]~6
Y[1]~4
Y[2]~5
Eo_L
GS_L~output
Eo_L~output
Y[1]~output
Y[2]~output
Y[3]~output
Y[0]~output
Y[0..3]
IO_OBUF
Chip 1
Chip 2
But it is better to run a gate-level simulation to measure propagation delays