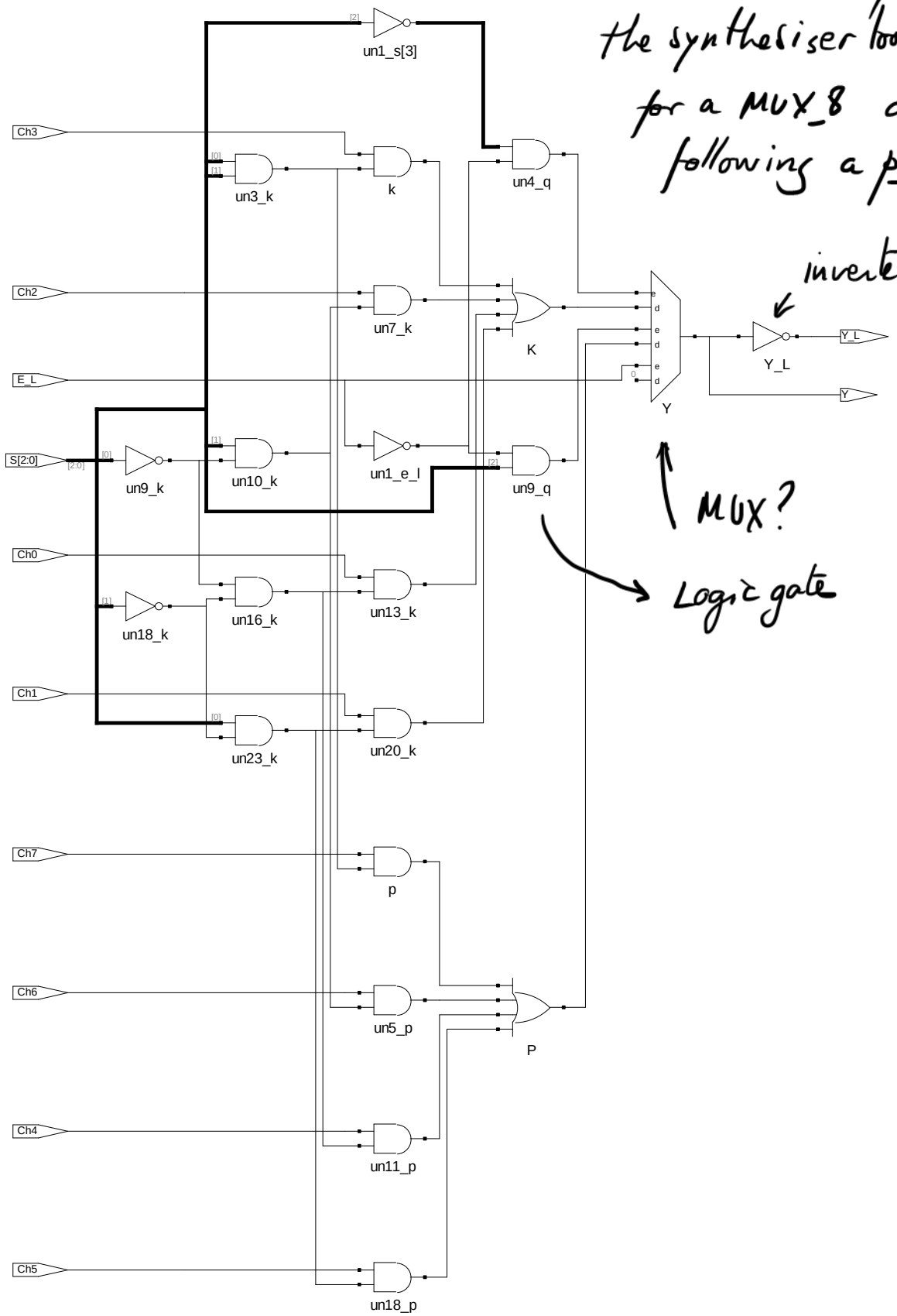
This is an ideal RTL schematic inveuted by the synthesiser tool for a MUX_8 described following a plan C1



inverters

MUX?

Logic gate

Plan C1 is not recommended. As you see, even if your circuit conception is hierarchical, the single file VHDL description produces a flat design like this one. Compare it with the RTL from plan C2.